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SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL

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Major Revisions in This Edition

Page	Revised points
CHAPTER 1	(1) Fine-pitch BGA package mouning pad dimension examples are added.
APPENDIX	(1) Fine-pitch BGA package daisy-chain wiring diagrams are added.
	(2) Reworking conditions of BGA package are added.
	(3) PWB layout is added.

CONTENTS

INTRODUCTION

As demands for electronic systems with the higher density has grown in recent years, packages used for semiconductor devices has become increasingly diversified.

Take IC products for example. Conventionally, DIP has been used as an internationally standard package, but it is expected that surface mount packages, such as QFP and SOP, which are more suitable for surface mounting, substantially grow.

To use these semiconductor devices in various shapes with a high reliability, developing and organizing the technology to mount the devices is extremely important.

Recently, soldering methods placing utmost emphasis on productivity, such as infrared reflow soldering and vapor phase soldering (VPS), have been increasingly employed as semiconductor device mounting technologies. With these technologies, semiconductor devices are subjected to a high temperature. Consequently, devices with excellent resistance to soldering heat and moisture resistance have been increasingly demanded.

This manual is intended to deepen the understanding by assembly manufacturers of the problems related to semiconductor devices and the mounting technologies, to provide general, but important information on handling semiconductor devices, and to introduce the mounting conditions recommended by NEC.

Surface mounting technology consists of various technologies, including component mounting technology, soldering technology, and cleaning technology, and have many problems as yet to be solved.

NEC intends to develop and establish technologies that improve the reliability of not only semiconductor devices but also their application systems, in close cooperation with mounting machine manufacturers, material manufacturers, component manufacturers, and assembly manufacturers.

In revising this document, examples of calculating the mounting pads for newly developed SMD packages and new examples of evaluation of mounting SMDs are added.

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NEC Corporation

[MEMO]

CHAPTER 1 SURFACE MOUNT SEMICONDUCTOR DEVICES (SMDs)

1.1 Features and Types of SMDs

1.1.1 Trend of SMDs

As the surface mount technology (SMT) has made a steady progress in recent years, electronic systems have increasingly become light weight, low-profile, and compact.

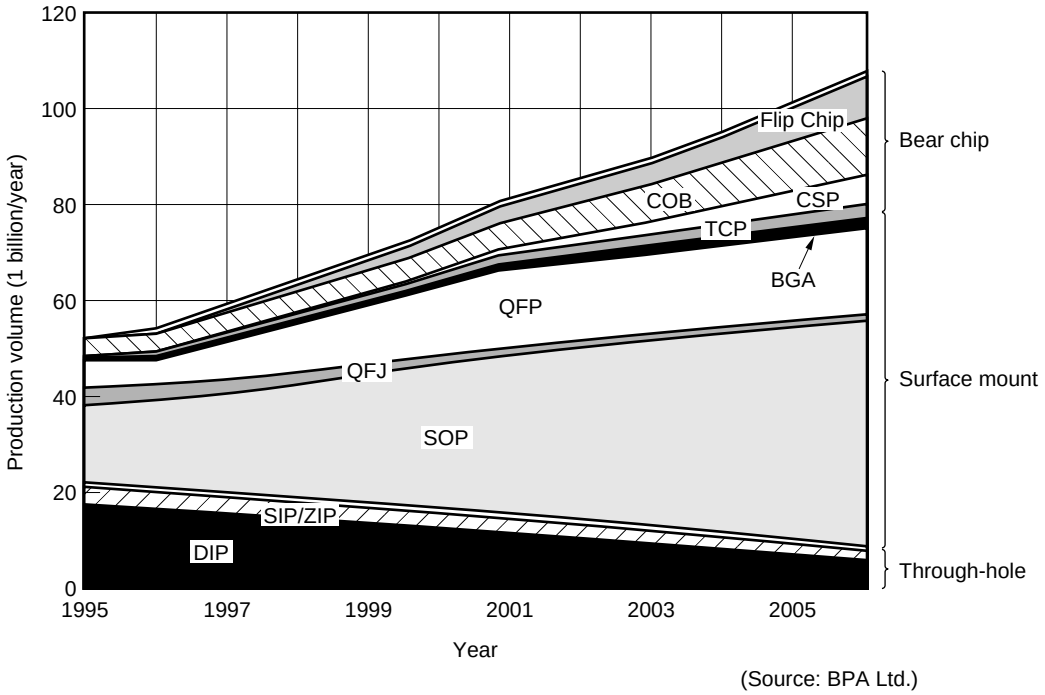
Against this background, semiconductor devices, which play a major role in high-density mounting technology, are increasingly incorporating slimmer package, more pins, and finer pin pitch, and surface mount type semiconductor devices (SMDs) (surface mount type) are now taking the place of the conventional, through-hole type devices (THDs) (pin insertion type) (hereafter, the surface mount devices are referred to as “SMDs” and through-hole devices are referred to as “THDs“ in this manual).

Recently, packages of the area array mounting type, which are suitable for high-density mounting, are receiving attention, and the production volume of BGA (ball grid array)-type packages are consequently increasing.

Figure 1-1 shows the projected production of various packages in the world.

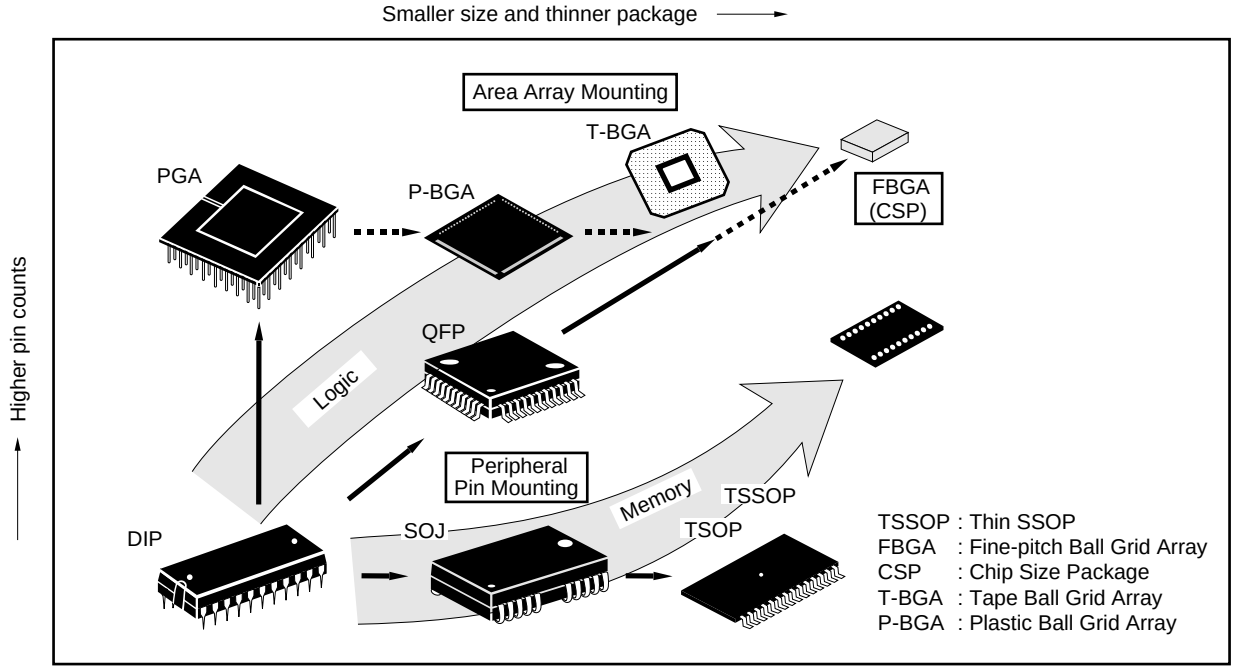
Figure 1-2 shows the trend in VLSI packages. As shown, the trend is toward slimmer packages, higher pin count, and fine pin pitch.

Figure 1-1. Projected Production of Different IC Packages (W/W)



(Source: BPA Ltd.)

Figure 1-2. VLSI Package Trend



1.1.2 Features of SMDs

The package of an SMD is provided with pins or metalized electrodes so that the device can be mounted on the surface of a printed wiring board (PWB).

Many pin shapes are available, including gull wing leads, J leads, and I leads (butt leads), solder balls.

An SMD package is designed to increase the density on the PWB, and has the following features:

(1) Merits

<1> Unlike THD packages, SMD packages can be mounted on both sides of a PWB.

<2> The wiring layout on a PWB can be substantially improved by using SMDs because no through-holes are necessary on the board, and mounting density can be increased.

<3> The cost for drilling can be reduced.

<4> Pin dimension can be shortened, and pitch can be made finer; consequently, stray capacitance and parasitic inductance can be reduced, and therefore, the operating speed can be improved.

<5> The cost for storage and transportation can be reduced because applications systems more compact and lighter in weight can be produced.

(2) Problems

<1> Because the pin pitch of SMD packages is much finer than that of the conventional THD packages (such as DIP), special care must be exercised in designing the PWB on which the SMDs are to be mounted, such as in designing foot patterns.

<2> SMDs are mounted by means of whole heating. Therefore, moisture absorption and soldering temperature of some SMDs must be controlled.

<3> SMDs have complicated, fine pins. This means that more sophisticated soldering technology is necessary and inspection after the SMDs have been mounted on a PWB must be conducted with higher accuracy.

<4> Because SMDs are designed to increase the density on a PWB, the board must be designed effectively to radiate heat (especially, when power devices are mounted).

1.1.3 Types of packages

Figure 1-3 shows the classification of semiconductor device packages. **Figure 1-4** classifies the packages of discrete components.

Figure 1-3. Classification of IC Packages

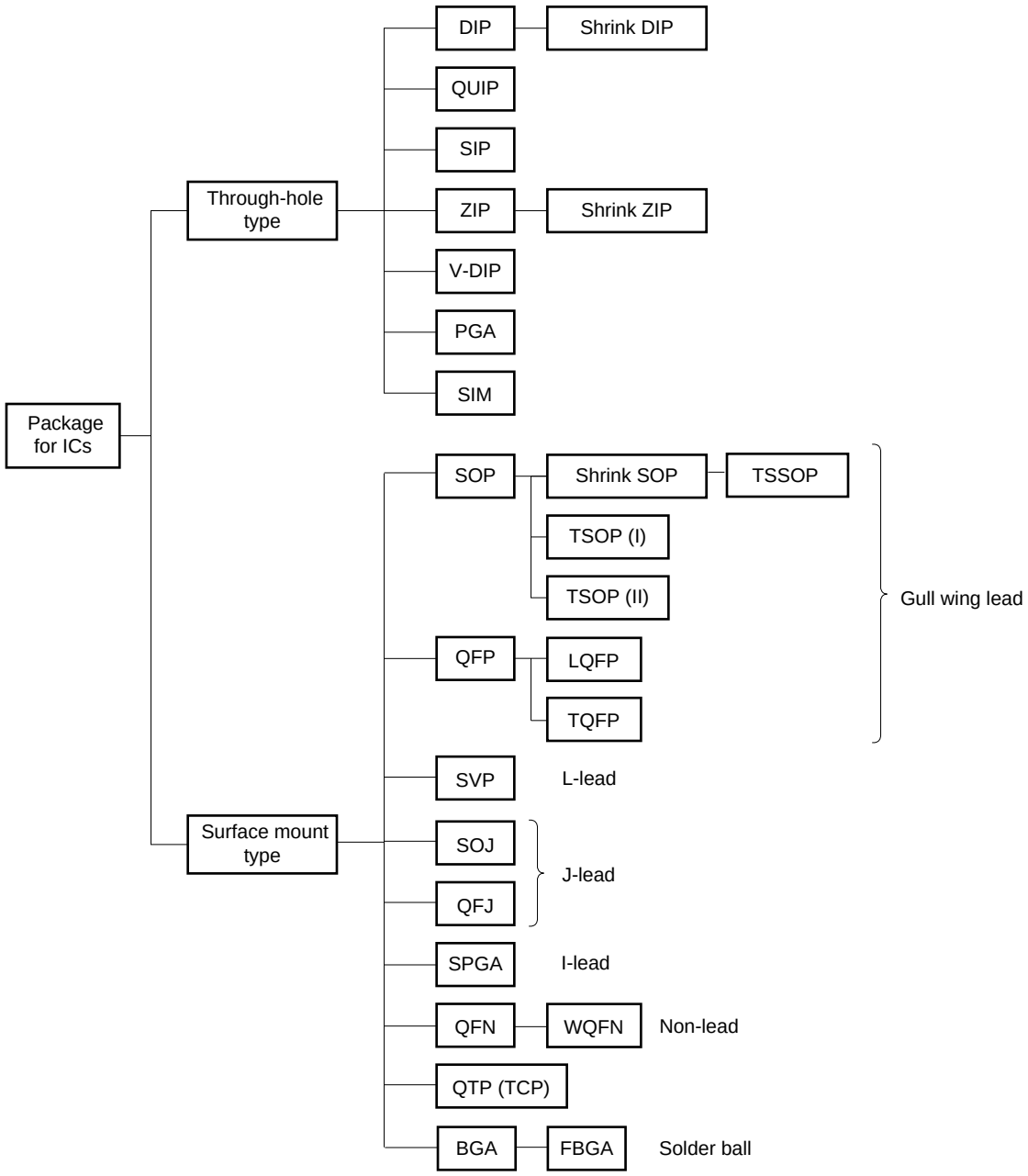
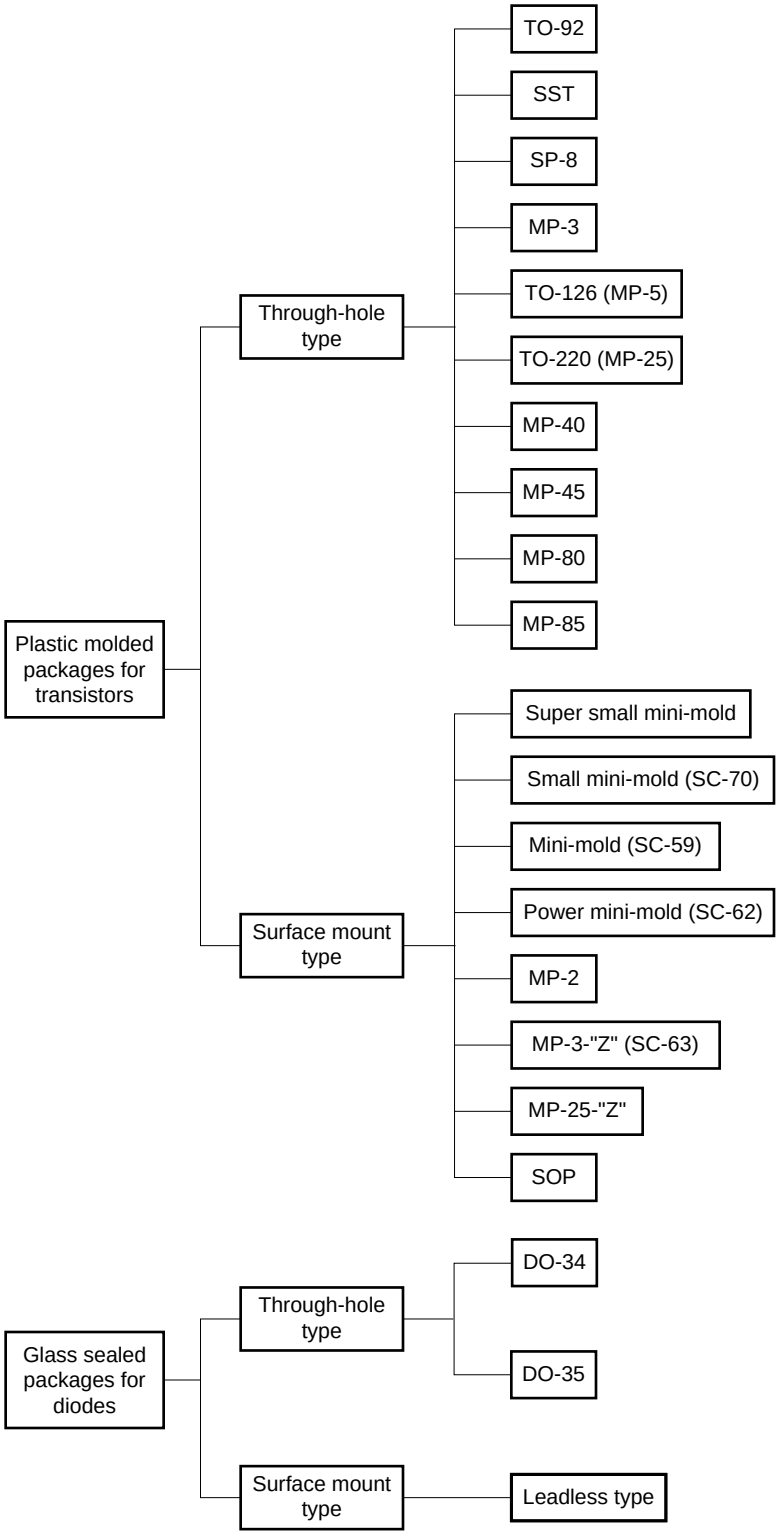


Figure 1-4. Classification of Discrete Device Packages



1.2 Mounting SMDs

1.2.1 Basic mounting flow

The flowchart shown in **Figure 1-5** illustrates how an SMD is basically mounted on a PWB.

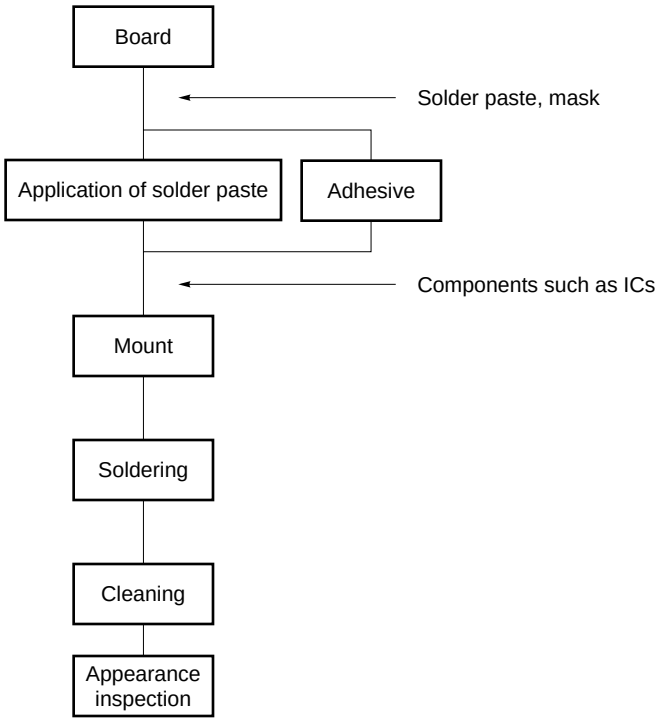
First, solder paste is applied to the locations on the PWB onto which the SMDs are to be soldered. Components, including SMDs, are placed on the PWB, and soldered by means of reflow soldering.

Sometimes, the solder paste is not used. Instead, components are temporarily fixed on the PWB with adhesive, and soldered.

After the components have been soldered, the PWB is cleaned for elimination of flux residues, solder balls, and other impurities, and the appearance of the components and PWB is inspected.

Each of these processes is described in detail from the next page.

Figure 1-5. Basic Mounting Flow



1.2.2 Designing PWB and pattern

(1) Selecting board

Many types of PWBs are available, such as copper-clad laminated PWBs made of paper phenol or glass epoxy, ceramic (aluminum) PWBs, and flexible boards of polyimide resin.
When selecting a PWB, the following points must be taken into account:

- Relations among components to be mounted and other materials in terms of thermal expansion coefficient
- Electrical characteristics
- Mechanical characteristics
- Thermal radiation characteristics
- Reliability
- Cost

At present, most of the electronic systems employ the copper-clad laminated PWBs, which can be classified as shown in **Table 1-1** by the substrate materials constituting the laminated board and resin. The basic dimensions of the PWB are 1 m $\times$ 1 m or 1.2 m $\times$ 1 m, and the thickness is 1.6 mm (including the thickness of the copper foil).
As the conductor materials, electrolytic copper foils with a thickness of 35 μm or 18 μm are usually used.

Table 1-1. Types of Laminated PWBs

Name	JIS No.	JIS Symbol
Copper-clad laminated PWB (paper substrate with epoxy resin)	JIS C6482	PE1F
Copper-clad laminated PWB (synthetic fiber substrate with epoxy resin)	JIS C6483	SE1
Copper-clad laminated PWB (glass substrate with epoxy resin)	JIS C6484	GE2, GE2F, GE4, GE4F
Copper-clad laminated PWB (paper substrate with phenol resin)	JIS C6485	PP3, PP3F, PP5, PP5F, PP7, PP7F

Generally, these PWBs are used as follows, depending on the applications:
The PWBs of glass substrate material with epoxy resin (GE4 or GE4F in the above table) are mainly used for industrial electronic systems (such as computers, electronic exchanges, OA equipment, wired communications equipment, radio communications equipment, various electronic systems, and electronic measuring instruments), and the boards of paper substrate material with phenol resin (PP3 through PP7) are used for consumer products (such as TVs, radios, tape recorders, and VCRs).
The glass epoxy laminated PWBs are excellent in electrical insulation, moisture resistance, and dimensional stability.
Although paper phenol PWBs are slightly inferior to epoxy boards in terms of performances, they are low-cost and easy to drill, and therefore, the copper-clad laminated PWBs are most frequently used.
In addition to these boards, flexible boards and ceramic boards are also used.
To mount fine-pitch SMDs and large-size SMDs, warped boards pose an extremely grave problem.
Generally, a warp of 1% or less in respect to the long side of the board is said to be acceptable. To mount a fine-pitch SMD, however, the warp must be 0.5 mm max./100 mm.

This must be also taken into consideration in mounting designing.

Table 1-2 shows the types of flexible copper-clad PWBs.

Table 1-2. Types of Flexible Boards

Substrate material	Substrate thickness (μm)	Width (mm) × length (m)	Remarks
Polyester film	25, 38, 50, 75, 100, 125	500 × (50 to 100)	Single-sided, copper-clad
Polyimide film	(12), 25, 50, 75, (125)	480 × (50 to 100)	Single-sided, copper-clad
Polyimide film	(12), 25, 50, 75	480 × 1.48 × 25	Double-sided, copper-clad
Glass epoxy	100	500 × (50 to 100)	Single-sided, copper-clad
Glass epoxy	100	500 × 1	Single-sided, double-sided

(2) Designing wiring pattern

In designing wiring patterns on a PWB, the external dimensions and the pin configuration of the SMD must be taken into consideration. In some cases, even SMDs with the same name (e.g., QFP) have slight differences in dimensions from one another. Especially, the pin length may vary depending on the application.

In addition, the wiring path and the wiring width from each pin considerably affect the mounting pad dimensions since the pins of BGA packages are placed in grids underneath the package.

This section describes how to design mounting pads, which have a significant influence on soldering quality and reliability.

When designing mounting pads, use the provided calculation examples as reference in determining the mounting density, mountability, and dimensional tolerance. For reference, the specifications of wiring width/interval of BGA packages\ are described in APPENDIX.

(a) Mounting pad of SOP

SOPs are named after the nominal center-to-center distance (e_1) between mounting pad arrays. Therefore, for example, the name “225 mils SOP” means that the center-to-center distance between the mounting pad arrays of this SOP is 225 mils (5.7 mm), as shown in **Figure 1-6**.

Therefore, the mounting pads for this SMD should be designed according to this center-to-center distance. With some packages, however, the center-line of the mounting pad arrays may not agree with the center of the flat portion of the pin (L). The reason for this is that the body dimensions or pin length slightly differs because of the development history of the package or functional differences.

Figure 1-6. Dimensions of SOP Mounting Pad

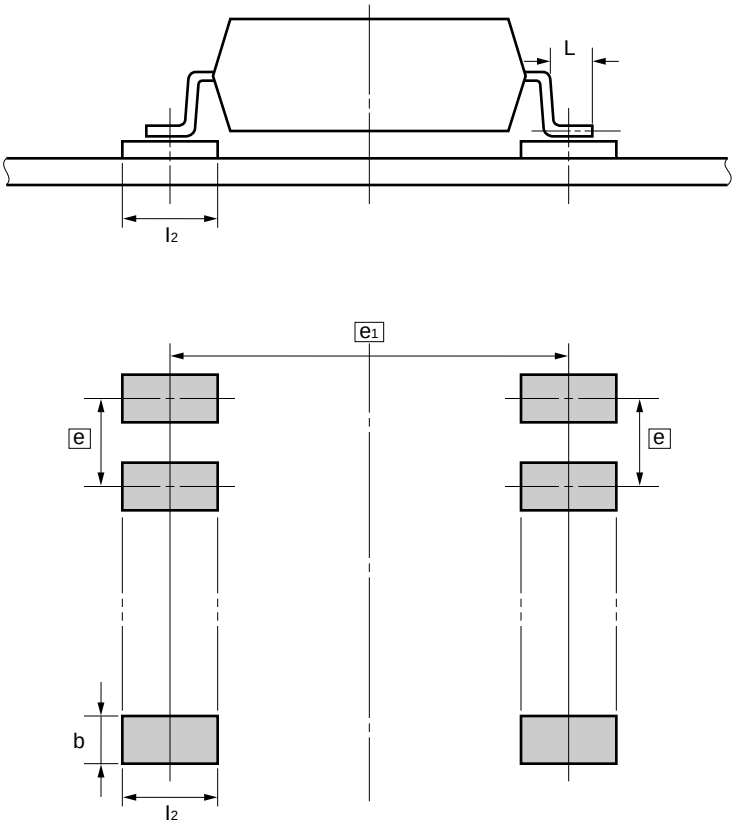


Table 1-3a. Example of Calculation of SOP Mounting Pad Dimensions

Unit: mm

Package		Nominal dimensions	Pin pitch	Pad dimensions	Pad length	Remarks
No. of pins	Code No.	e_1	e	b	l_2	
8	S8GM-50-225B-4	5.72 (225 mils)	1.27	0.76	1.27	Plastic SOP
14	S14GM-50-225B, C-4					
16	S16GM-50-255B, C-4					
8	P8GM-50-300B-3	7.62 (300 mils)				
14	P14GM-50-300B-4					
16	P16GM-50-300B-4					
20	P20GM-50-300B, C-4					
24	P24GM-50-300B-4					
16	P16GM-50-375A-2 P16GM-50-375B-3 P16GT-50-375B	9.53 (375 mils)				
20	P20GM-50-375B-4 P20GT-50-375B-1					
24	P24GM-50-375B-3 P24GT-50-375B-1					
28	P28GM-50-375B-3 P28GT-50-375B-1					
24	P24GM-50-450A-2	11.43 (450 mils)				
28	P28GM-50-450A1-2 P28GM-50-450A2-2 P28GU-50-450A-1					
32	S32GM-50-525A-2 P32GW-50-525A	13.34 (525 mils)				
40	P40GW-50-525A					
44	P44GX-50-600A-1 P44GX-50-600A1-1	15.24 (600 mils)				
32	P32BW-50-525A-2 P32BW-50-525A1-3 P32BW-50-525A2 P32BW-50-525A3	13.34 (525 mils)				Ceramic WSOP

Notes 1. The mounting pad dimensions in this table correspond to the packages identified by the dimension code No. For the detailed dimensions of each package, refer to the Data Sheet of your product, or “Semiconductor Device Package Manual (C10943X)”.

2. In actual designing, optimization is necessary taking various factors such as mounting density, mountability, and dimensional tolerances into consideration.

Table 1-3b. Example of Calculation of Shrink SOP Mounting Pad Dimensions

Unit: mm

Package		Nominal dimensions	Pin pitch	Pad dimensions	Pad length
No. of pins	Code No.	e_1	e	b	l_2
14	P14GM-65-225B-2	5.72	0.65	0.35	1.27
16	P16GM-65-225B-2	(225 mils)			
20	P20GR-65-225C-1				
20	P20GM-65-300B-2	7.62			
24	P24GS-65-300B-1	(300 mils)			
30	P30GS-65-300B-1				
30	S30GS-80-300C		0.80	0.50	
36	P36GM-80-300B-3				
38	P38GS-65-300B-1		0.65	0.35	
30	S30GT-65-375B	9.53	0.65	0.35	1.30
38	P38GT-65-375B	(375 mils)			1.27
42	S42GT-80-375B-1		0.80	0.50	1.30
48	P48GT-65-375B-1		0.65	0.35	1.27
64	P64GW-80-525A-1	13.34 (525 mils)	0.80	0.50	

Notes 1. The mounting pad dimensions in this table correspond to the packages identified by the dimension code No. For the detailed dimensions of each package, refer to the Data Sheet of your product, or “Semiconductor Device Package Manual (C10943X)”.

2. In actual designing, optimization is necessary taking various factors such as mounting density, mountability, and dimensional tolerances into consideration.

(b) Mounting pad of TSSOP

The nominal dimensions of the TSSOP (thin shrink SOP) are determined by the width of the plastic body (E).

In designing the mounting pads of this package, therefore, the body width (E) and pin dimensions (length of soldered portion: Lp, length of flat potion of pin: L) are important.

Although these pin dimensions should be standardized in order to standardize the mounting pads, they differ slightly depending on the manufacturer.

Design the mounting pad of the TSSOP as follows:

Determine the mounting pad dimensions by using the expressions shown in Figure 1-7.

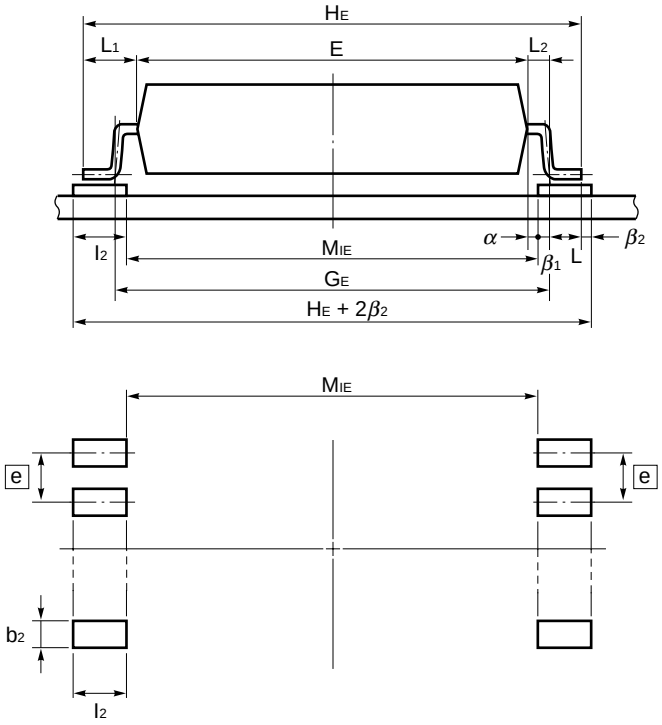
First, determine the package length range (inner length between the flat portions of pins) G_E from the total width H_E and the length of the soldered portion L_{pmax}. Next, determine the mounting length M_{IE} from the G_{Emin} obtained and constant β_1.

Next, determine the mounting pad length l_2 from the total length H_E, constant β_2, and M_{IE}. If emphasis is placed on the soldering strength, constant β_1 should be 0.1 mm, taking the package length range (inner length between the flat portions of pins) G_E into account. Constant β_2 is generally 0.2 mm or more, taking the pattern accuracy of the solder paste screen and easiness of visible inspection of soldering into account.

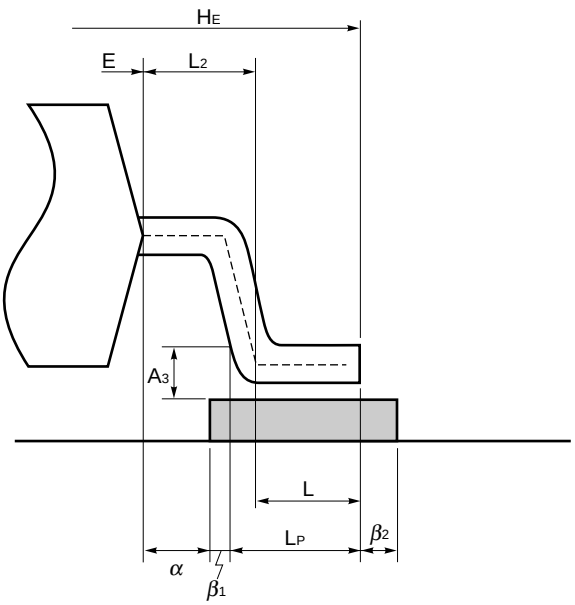
Generally, α = 0.1 mm if easiness of cleaning is taken into consideration. Add constant α to body width E_{MAX} to determine the mounting length M_{IE}. The pad length must therefore be designed according to your mounting conditions.

The mounting pad width b_2 is determined by pin width b, pin pitch e, and γ. The value of γ is generally 0.25 mm to prevent the generation of solder bridges.

Figure 1-7. Mounting Pad Dimensions of TSSOP



<Enlargement>



$G_{E(MIN)} = H_{E(MIN)} - 2L_{PMAX}$ α = 0.1 mm

$M_{IE} = G_{E(MIN)} - 2\beta_1$ β_1 = 0.1 mm

$l_2 \geq (H_{E(MAX)} + 2\beta_2 - M_{IE})/2$ β_2 = 0.2 mm

$b \leq b_2 \leq \boxed{e} - \gamma$ γ = 0.3 mm

Table 1-3c. Example of Calculation of TSSOP Mounting Pad Dimensions

Unit: mm

Package		Nominal dimensions	Pin pitch	Mounting width	Pad width	Pad length	Remarks
No. of pins	Code No.	e_1	e	M_1	b	l_2	
8	S8GR-65-9JG	225 mils	0.65	4.5	0.35	1.25	
20	S20GS-65-300B	300 mils	0.65	6.2	0.35	1.25	
26	S26GS-50-9JH	300 mils	0.5	6.2	0.25	1.25	

(c) Mounting pad of TSOP (type I)

The nominal dimensions of the TSOP (thin small outline package) (type I) are determined by the combination of the width of the plastic body (E) and the total length (H_D).

For example, "32-pin 8 × 20 TSOP (type I)" means that the package width is 8 mm, and that the total length (including the pins) is 20 mm.

In designing the mounting pads of this package, therefore, the body length (D) and pin dimensions (pin length: L1, length of flat portion of pin: L or length of soldered portion L_p) are important.

The length of soldered portion L_p is established with the recent EIAJ specifications to be a dimensional value that allows dimensional measurement more accurate than that using the length of flat portions of pins L and takes the fillet formation, which affects soldering reliability, into consideration. The L_p dimensional notation has been adopted starting from newly-developed packages.

Although these pin dimensions should be standardized to standardize mounting pads, they slightly differ depending on the manufacturer.

Design the mounting pads of the TSOP (type I) as follows:

Determine the mounting pad dimensions by using expression a in Figure 1-8a when only the length of the flat portion of pins L is indicated in the package outline.

First, determine the package length range (inner length between the flat portions of pins) G_D from the total length H_D and the pin length L_{pmax}. Next, determine the mounting length M_{ID} from the G_{Dmin} obtained and constant β_1.

Next, determine the mounting pad length l_2 from the total length H_D, constant β_2, and M_{ID}.

If emphasis is placed on the soldering strength, constant β_1 should be 0.2 mm, taking the package length range (inner length between the flat portions of pins) G_D into account. Constant β_2 is generally 0.2 mm or more, taking the pattern accuracy of the solder paste screen and easiness of visible inspection of soldering into account.

Determine the mounting pad dimensions by using expression b in Figure 1-8a when the length of flat portions of pins L and the length of soldered portion L_p are indicated in the package outline.

First, determine the package length range (inner length between the flat portions of pins) G_D from the total length H_D and the pin length L_{pmax}. Next, determine the mounting length M_{ID} from the G_{Dmin} value obtained and constant β_1.

Next, determine the mounting pad length l_2 from the total length H_D, constant β_2, and M_{ID}.

If an emphasis is placed on the soldering strength, constant β_1 should be 0.1 mm, taking the package length range (inner length between the flat portions of pins) G_D into account. Constant β_2 is generally 0.2 mm or more, taking the pattern accuracy of the solder paste screen and easiness of visible inspection of soldering into account.

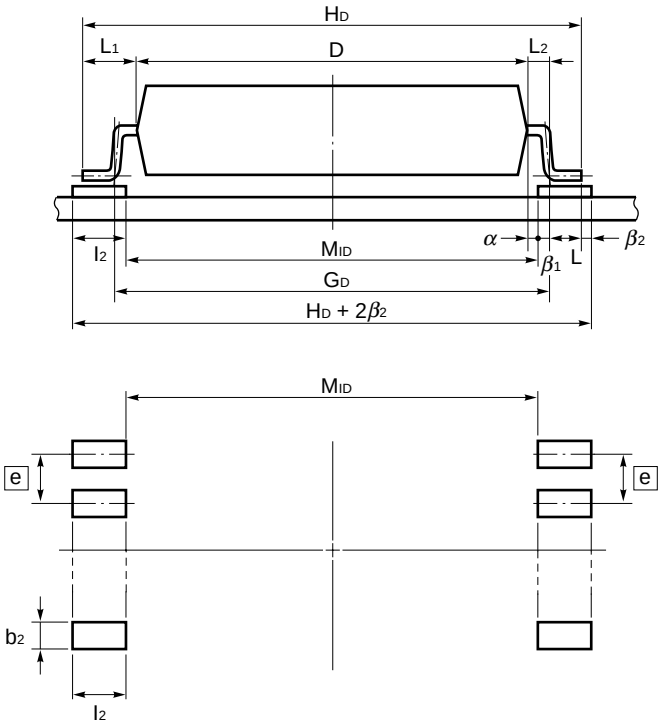
Generally, α = 0.1 mm if easiness of cleaning is taken into consideration. Add constant α to body length D_{MAX} to determine the mounting length M_{ID}.

The pad length must therefore be designed according to your mounting conditions.

The mounting pad width b_2 is determined by pin width b, pin pitch e, and γ. The value of γ is generally 0.25 mm to prevent the generation of solder bridges.

Described above is the guideline of dimensions for TSOP (type I) whose pin pitch is 0.5 mm. For fine-pitch TSOP (type I) whose pin pitch is less than 0.5 mm, the value of γ must be smaller.

Figure 1-8a. Mounting Pad Dimensions of TSOP (Type I)



(Expression a)

$G_{D(MIN)} = H_{D(MIN)} - 2L_{(MAX)}$

$M_{ID} = G_{D(MIN)} - 2\beta_1$

$I_2 \geq (H_{D(MAX)} + 2\beta_2 - M_{ID})/2$

$b \leq b_2 \leq \boxed{e} - \gamma$

α = 0.1 mm

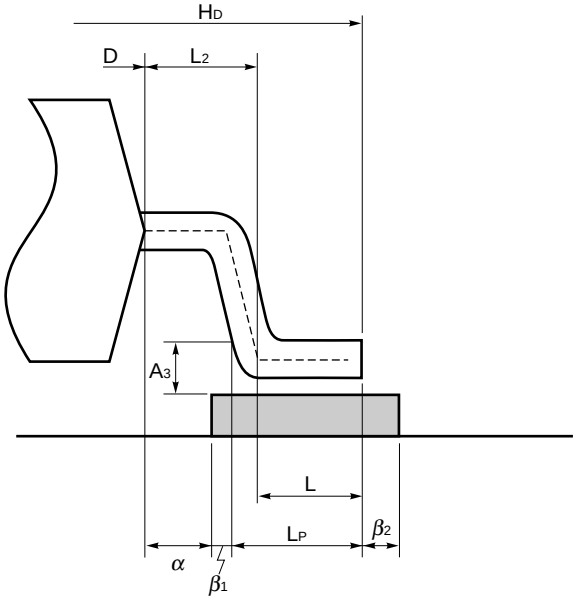
β_1 = 0.2 mm

β_2 = 0.2 mm

γ = 0.25 mm ($\boxed{e}$ = 0.5)

0.20 mm ($\boxed{e}$ = 0.4)

0.15 mm ($\boxed{e}$ = 0.3)



(Expression b)

$G_{D(MIN)} = H_{D(MIN)} - 2L_{PMAX}$

$M_{ID} = G_{D(MIN)} - 2\beta_1$

$I_2 \geq (H_{D(MAX)} + 2\beta_2 - M_{ID})/2$

$b \leq b_2 \leq \boxed{e} - \gamma$

α = 0.1 mm

β_1 = 0.1 mm

β_2 = 0.2 mm

γ = 0.25 mm ($\boxed{e}$ = 0.5)

Table 1-4a. Example of Calculation of TSOP (Type I) Mounting Pad Dimensions

Unit: mm

Package		Body width	Total length	Pin pitch	Mounting width	Pad width	Pad length
No. of pins	Code No.	E	H_D	e	M_{ID}	b	l_2
24	S24GX-50-JJH-2 S24GX-50-JKH-2	6.0	16.0	0.50	14.2	0.25	1.2
28	P28GW-55-9JL-1 P28GW-55-9KL-1	8.0	13.4	0.55	11.6		
32	S32GX-50-EJA-1 S32GX-50-EKA-1	8.0	15.3 (600 mils)	0.50	13.5		
	S32GZ-50-KJH-3 S32GZ-50-KKH-3		20.0		18.2		
	P32GU-50-9JH P32GU-50-9KH		13.4		11.5		1.25
40	S40GZ-50-LJH-2 S40GZ-50-LKH-2	10.0	20.0		18.2		1.2
48	S48GY-50-MJH-2 S48GY-50-MKH-2	12.0	18.0		16.2		

Notes 1. The mounting pad dimensions in this table correspond to the packages identified by the dimension code No. For the detailed dimensions of each package, refer to the Data Sheet of your product, or "Semiconductor Device Package Manual (C10943X)".

2. In actual designing, optimization is necessary taking various factors such as mounting density, mountability, and dimensional tolerances into consideration.

(d) Mounting pad of TSOP (type II)

The nominal dimensions of TSOP (thin small outline package) (type II) are determined by the plastic body width (E).

In designing the mounting pads of this package, therefore, the body width (E) and pin dimensions (pin length: L1, length of flat portion of pin: L or length of soldered portion L_p) are important.

The length of soldered portion L_p is established with the recent EIAJ specifications to be a dimensional value that allows dimensional measurement more accurate than that using the length of flat portions of pins L and takes the fillet formation, which affects soldering reliability, into consideration. The L_p dimensional notation has been adopted starting from newly-developed packages.

Although these pin dimensions should be standardized to standardize mounting pads, they slightly differ depending on the manufacturer.

Design the mounting pads of the TSOP (type II) as follows:

Determine the mounting pad dimensions by using expression a in Figure 1-8b when only the length of the flat portions of pins L is indicated in the package outline.

First, determine the package width range (inner length between the flat portions of pins) G_E from the total width H_E and the pin length L_{max}. Next determine the mounting length M_{IE} from the G_{Emin} obtained and constant β_1.

Next determine the mounting pad length l_2 from the total width H_E, constant β_2, and M_{IE}.

If emphasis is placed on the soldering strength, constant β_1 should be 0.2 mm, taking the package width range (inner length between the flat portions of pins) G_E into account. Constant β_2 is generally 0.2 mm or more, taking the pattern accuracy of the solder paste screen and easiness of visible inspection of soldering into account.

Determine the mounting pad dimensions by using expression b in Figure 1-8b when the length of flat portion of pins L and the length of soldered portions L_P are indicated in the package outline.

First, determine the package length range (inner length between the flat portions of pins) G_D from the total length H_D and the pin length L_{pmax}. Next determine the mounting length M_{ID} from the G_{Dmin} value obtained and constant β_1.

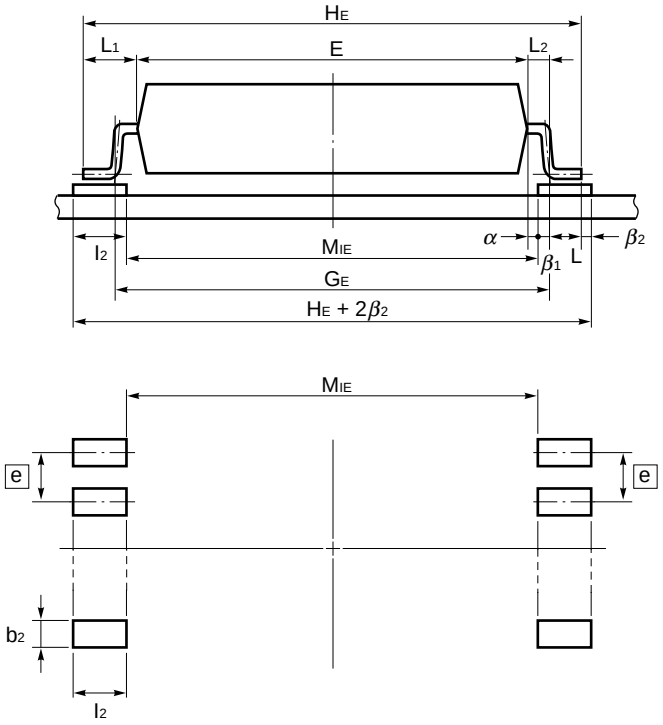
Next determine the mounting pad length l_2 from the total length H_D, constant β_2, and M_{ID}.

If an emphasis is placed on the soldering strength, constant β_1 should be 0.1 mm, taking the package length range (inner length between the flat portions of pins) G_D into account. Constant β_2 is generally 0.2 mm or more, taking the pattern accuracy of the solder paste screen and easiness of visible inspection of soldering into account.

Generally, α = 0.1 mm if easiness of cleaning is taken into consideration. Add constant α to body width E_{MAX} to determine the mounting length M_{IE}. In this case, however, the connection strength may be deteriorated because the dimension of β_1 is short. The pad length must therefore be designed according to your mounting conditions.

The mounting pad width b2 is determined by pin width b, pin pitch e, and γ. The value of γ is generally 0.3 mm to prevent the generation of solder bridges.

Figure 1-8b. Mounting Pad Dimensions of TSOP (Type II)



(Expression a)

$G_{E(MIN)} = H_{E(MIN)} - 2L_{MAX}$

$M_{IE} = G_{E(MIN)} - 2\beta_1$

$l_2 \geq (H_{E(MAX)} + 2\beta_2 - M_{IE})/2$

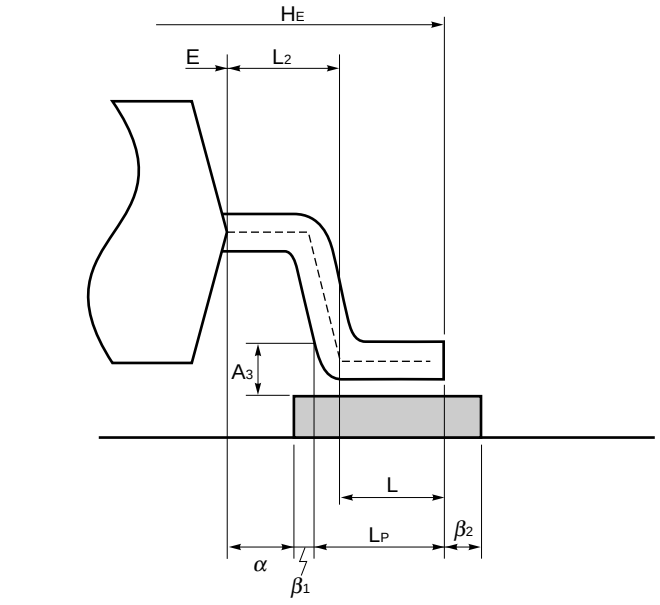
$b \leq b_2 \leq e - \gamma$

α = 0.1 mm

β_1 = 0.2 mm

β_2 = 0.2 mm

γ = 0.3 mm



(Expression b)

$G_{E(MIN)} = H_{E(MIN)} - 2L_{PMAX}$

$M_{IE} = G_{E(MIN)} - 2\beta_1$

$l_2 \geq (H_{E(MAX)} + 2\beta_2 - M_{IE})/2$

$b \leq b_2 \leq e - \gamma$

α = 0.1 mm

β_1 = 0.1 mm

β_2 = 0.2 mm

γ = 0.3 mm

Table 1-4b. Example of Calculation of TSOP (Type II) Mounting Pad Dimensions (1/2)

Unit: mm

Package		Body width	Body length	Pin pitch	Mounting width	Pad width	Pad length
No. of pins	Code No.	$E_{(MAX)}$	$D_{(MAX)}$	e	M_{ID}	b_2	l_2
26	S26GS-50-9JD-2	7.72 (300 mils)	17.54	1.27	7.42	0.7	1.2
	S26GS-50-9KD-2						
	S26G3-50-7JD-1		17.4				
	S26G3-50-7KD-1						
	S26G3-50-7JD1		17.36				
	S26G3-50-7KD1						
	S26G3-50-9JD						
	S26G3-50-9KD						
28	S28G5-50-7JD-2	10.26 (400 mils)	18.81		9.96		
	S28G5-50-7KD-2						
	S28G5-50-7JD1-1						
	S28G5-50-7KD1-1						
	S28G5-50-7JD2-1						
	S28G5-50-7KD2-1						
	S28G5-50-7JD3		18.63				
	S28G5-50-7KD3						
	S28G5-50-7JD4						
	S28G5-50-7KD4						
	S28G5-50-7JD5						
	S28G5-50-7KD5						
32	S32G5-50-7JD-2		21.17				
	S32G5-50-7KD-2						
	S32G5-50-7JD1-1						
	S32G5-50-7KD1-1						
	S32G5-50-7JD2						
	S32G5-50-7KD2						
44	S44G5-80-7JF-1		18.81	0.80		0.5	
	S44G5-80-7KF-1						
	S44G5-80-7JF1-1						
	S44G5-80-7KF1-1						
	S44G5-80-7JF2		18.63				
	S44G5-80-7KF2						
	S44G5-80-7JF3						
	S44G5-80-7KF3						
	S44G5-80-7JF4						
	S44G5-80-7KF4						
	S44G5-80-7JF5						
	S44G5-80-7KF5						

Note 1. The mounting pad dimensions in this table correspond to the packages identified by the dimension code No. For the detailed dimensions of each package, refer to the Data Sheet of your product, or "Semiconductor Device Package Manual (C10943X)".

Note 2. In actual designing, optimization is necessary taking various factors such as mounting density, mountability, and dimensional tolerances into consideration.

Table 1-4b. Example of Calculation of TSOP (Type II) Mounting Pad Dimensions (2/2)

Unit: mm

Package		Body width	Body length	Pin pitch	Mounting width	Pad width	Pad length
No. of pins	Code No.	$E_{(MAX)}$	$D_{(MAX)}$	e	M_{ID}	b_2	l_2
50	S50G5-80-7JF-1	10.26 (400 mils)	21.45	0.80	9.96	0.5	1.2
	S50G5-80-7KF-1						
	S50G5-80-7JF1				9.46		
	S50G5-80-7KF1						
	S50G5-80-7JF2		21.17				
	S50G5-80-7KF2						
	S50G5-80-7JF3						
	S50G5-80-7KF3						
	S50G5-80-7JF4						
	S50G5-80-7KF4						
54	S54G5-80-9JF		22.62		9.96		
70	S70G5-65-7JG		24.29	0.65			
	S70G5-65-7KG						
	S70G5-65-7JG1				9.86		1.25
	S70G5-65-7KG1						
34	S34G7-50-7JD	12.7 (500 mils)	22.66	1.27	12.5	0.7	1.2
	S34G7-50-7KD						
54	S54G7-80-7JF			0.80		0.5	
	S54G7-80-7KF						
48	S48G8-80-7JF-1	14.07 (500 mils)	20.52		13.77		
	S48G8-80-7KF-1						

Note 1. The mounting pad dimensions in this table correspond to the packages identified by the dimension code No. For the detailed dimensions of each package, refer to the Data Sheet of your product, or "Semiconductor Device Package Manual (C10943X)".

Note 2. In actual designing, optimization is necessary taking various factors such as mounting density, mountability, and dimensional tolerances into consideration.

(e) Mounting pad of QFP

The nominal dimensions of QFP (quad flat package) are determined by the dimensions of the plastic body. For example, "64-pin 14 × 20 QFP" means that the body dimensions are 14 mm × 20 mm. In designing the mounting pads of this package, therefore, the body dimensions and pin dimensions (pin pull-out length: L_2, length of flat portion of pin: L) are important.

Although these pin dimensions should be standardized in order to standardize the mounting pads, they differ slightly depending on the manufacturer at present.

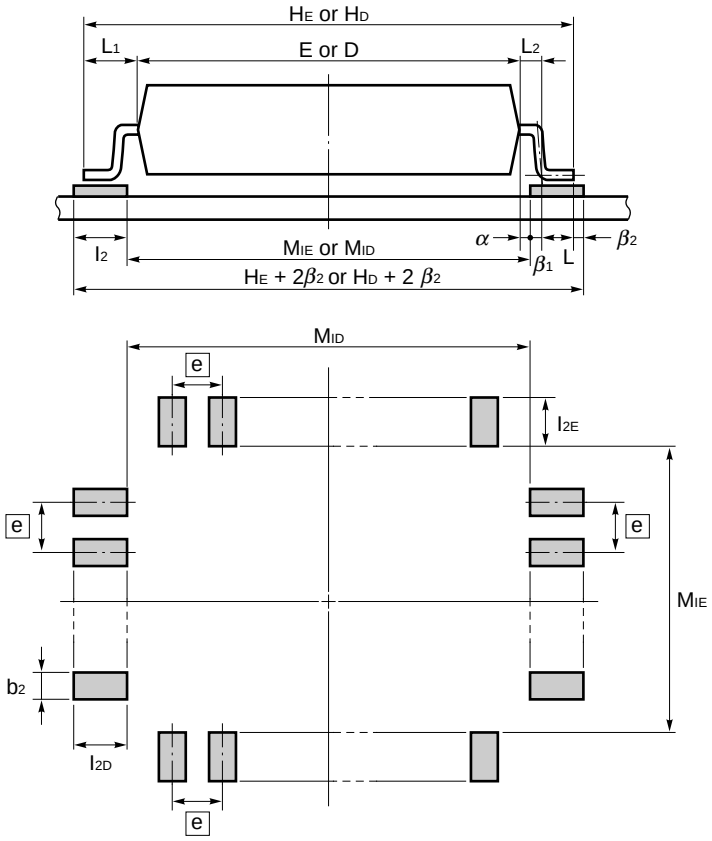
Design the mounting pads of the QFP as follows:

Determine the mounting pad dimensions by using the expressions shown in **Figure 1-9**.

Since the body dimensions are known, add constant α to these dimensions to determine mounting widths M_{ID} and M_{IE}. Next, determine the mounting pad length l_2 from the length of flat portion of the pin, L, and constants β_1 and β_2.

Generally, α is 0.2 mm if easiness of cleaning is taken into consideration. β_1 is 0.5 mm, taking solder strength into consideration, and β_2 is 0.2 mm or more, taking the pattern accuracy of the solder paste screen and easiness of visual inspection of soldering into account. Mounting pad width b_2 is determined by pin width b, pin pitch $\boxed{e}$, and constant γ. The value of γ is generally 0.3 mm to prevent generation of solder bridges. The above description applies to QFPs with a pin pitch of 0.65 mm or more.

Figure 1-9. Mounting Pad Dimensions of QFP



$M_{IE} = E_{(MAX.)} + 2\ \alpha$ α = 0.2 mm

$M_{ID} = D_{(MAX.)} + 2\ \alpha$ β_1 = 0.5 mm

$l_{2D} \geqq (H_{D(MAX.)} + 2\ \beta_2 - M_{ID})\ /2$ β_2 = 0.2 mm

$l_{2E} = (H_{E(MAX.)} + 2\beta_2 - M_{IE})\ /2$

$b \leqq b_2 \leqq e - \gamma$ γ = 0.3 mm

Note $E_{(MAX.)}$, $D_{(MAX.)}$, $H_{E(MAX.)}$, and $H_{D(MAX.)}$ are the maximum values including tolerances.

Table 1-5a. Example of Calculation of QFP Mounting Pad

Unit: mm

Package		Body width E	Body length D	No. of pins/side		Pin pitch e	Mounting width		Pad width b_2	Pad length l_2
No. of pins	Code No.			n_E	n_D		M_{IE}	M_{ID}		
40	P40G-80-F-2	9.5		10		0.8	10.1		0.5	2.1
44	P44G-80-22-2	10.0		11		0.8	10.6		0.5	1.9
	P44G-80-24-2									1.9
	P44GB-80-3B4-3									1.9
	S44GB-80-3B4-2									1.7
	S44GB-80-3BS									1.6
48	P48GB-65-2A5-3	10.0		12		0.65	10.6		0.35	1.5
	P48GH-80-2A5-4	10	14	10	14	0.8	10.6	14.6	0.5	1.5
52	P52G-100-00-2	14		13		1	14.6		0.7	3.6
	P52G-100-04-2									3.4
	P52G-100-05-1									2.2
	P52G-100-22-2									2.3
	P52G-100-24-2									2.3
	P52GC-100-3B6, 3BH-2									1.9
	S52GC-100-3BH-3									1.6
	P52GC-100-AB6-4									1.9
54	P54G-65-F-2	9.5		14	13	0.65	10.1		0.35	2.1
	P54G-65-R-2									2.1
56	S56GB-65-1A7-3	10		14		0.65	10.6		0.35	1.5
	P56GB-65-1P7-1									1.5
	S56GB-65-3B7-3									1.7
	S56GH-80-3B7-2	10	14	12	16	0.8	10.6	14.6	0.5	1.7
58	P58G-100-10-2	10.6	20.2	10	19	1	11.2	20.8	0.7	2.2
64	S64GF-100-3B8, 3BE-3	14	20	13	19	1	14.6	20.6	0.7	1.7
	P64G-100-F-2									2.45
	P64G-100-12, 1B-2									2.45
	P64GF-100-3B8, 3BE, 3BR-2									1.9
	P64G-100-14-2									2.2
	P64G-80-22-2	14		16		0.8	14.6		0.5	2.3
	P64GC-80-AB8-3									1.9
	P64GC-80-3BE-2									1.9
	S64GC-80-3BE-2									1.9
	P64GK-65-8A8-1	12		16		0.65	12.6		0.35	1.5

Package		Body width E	Body length D	No. of pins/side		Pin pitch	Mounting width		Pad width	Pad length
No. of pins	Code No.			n_E	n_D	e	M_{IE}	M_{ID}	b_2	l_2
68	S68GH-65-2AK-2	10	14	14	20	0.65	10.6	14.6	0.35	1.5
74	S74GJ-100-5BJ-3	20		18		1	20.6		0.7	1.7
80	P80G-80-1C-2	14	20	16	24	0.8	14.6	20.6	0.5	2.45
	P80GF-80-3B9-3									1.9
	S80GC-80-02-2			13	19					2.1
	P80GC-80-12-2									2.45
	S80GF-80-3B9-3			16	24					1.7
	S80GC-65-3B9-4	14		20		0.65	14.6		0.35	1.7
	S80GC-65-7ET-2						14.5		0.5	1.9
	P80GC-65-8BT						14.6		0.35	1.6
94	S94GJ-80-5BG-3	20		24		0.8	20.6		0.5	1.7
100	P100G-65-10-2	14.0	20.0	20	30	0.65	14.6	20.6	0.35	2.9
	P100G-65-12-2									2.45
	P100GF-65-3BA-3									1.9
	P100GF-65-3BA1-2									1.9
	S100GF-65-3BA-3									1.7
	S100GF-65-JBT									1.7
	S100GF-65-8ET						13.8	19.8		1.4
120	P120GD-80-5BB-3	28		30		0.8	28.6		0.5	2.1
	P120GD-80-LBB, MBB-1									
136	P136GD-65-5BC-3			34		0.65			0.35	
160	P160GD-65-5BD-3			40						
	P160GD-65-LBD, MBD									
	S160GD-65-LGD, MGD									1.6
184	P184GN-65-LGT-1			46			32.6			1.7
208	S208GL-65-6GL-1			52			40.6			1.7

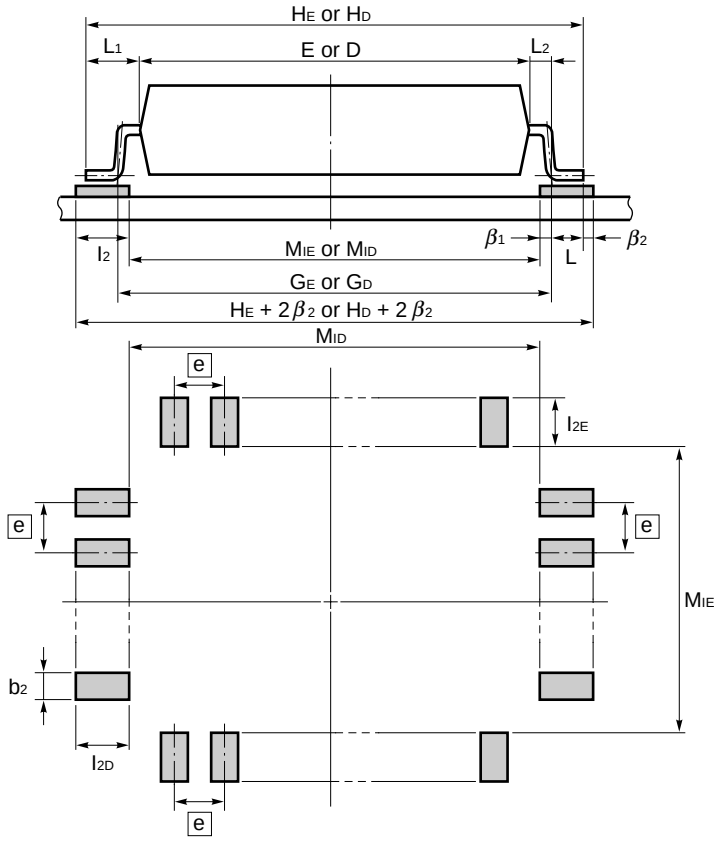
Notes 1. The mounting pad dimensions in this table correspond to the packages identified by the dimension code No. For the detailed dimensions of each package, refer to the Data Sheet of your product, or "Semiconductor Device Package Manual (C10943X)".

2. In actual designing, optimization is necessary taking various factors such as mounting density, mountability, and dimensional tolerances into consideration.

(f) Mounting pad of fine-pitch QFP

The nominal dimensions of a fine-pitch QFP are determined by the plastic body dimensions.
In designing the mounting pads of this package, therefore, the body dimensions and pin dimensions (pin pull-out length: L_2, length of flat portion of pin: L, pin width: D) are important.
Although these pin dimensions should be standardized in order to standardize the mounting pads, they slightly differ depending on the manufacturer at present.
Design the mounting pads of the fine-pitch QFP as follows:
Determine the mounting pad dimensions by using the expressions shown in **Figure 1-10**.
First, determine the package width range (inner length between the flat portions of pins) G_E from the total width H_E and pin length L_{max}. Next determine the mounting length M_{IE} from the G_{Emin} obtained and constant β_1. Next, determine the mounting pad length I_2 from the total width H_E, constant β_2, and M_{IE}.
If an emphasis is placed on the solder strength, constant β_1 should be 0.3 mm, taking the package width range (inner length between the flat portions of pins) G_E into account.
β_2 is generally 0.2 mm or more, taking the pattern accuracy of the solder paste screen and easiness of visible inspection of soldering into account.
The mounting pad width b_2 is determined by pin width b, pin pitch $\boxed{e}$, and constant γ. The value of γ is set to prevent the generation of solder bridges.

Figure 1-10. Mounting Pad Dimensions of Fine-Pitch QFP



$G_{E(MIN.)} = H_{E(MIN.)} - 2L_{MAX}$

$G_{D(MIN.)} = H_{D(MIN.)} - 2L_{MAX}$

$M_{IE} = G_{E(MIN.)} - 2\beta_1$

$M_{ID} = G_{D(MIN.)} - 2\beta_1$

$l_{2E} \geqq (H_{E(MAX.)} + 2\beta_2 - M_{IE})/2$

$l_{2D} \geqq (H_{D(MAX.)} + 2\beta_2 - M_{ID})/2$

$b \leqq b_2 \leqq e - \gamma$

$\beta_1 = 0.3$ mm

$\beta_2 = 0.2$ mm

$\gamma = 0.25$ ($e = 0.5$ mm)

0.20 ($e = 0.4$ mm)

Table 1-5b. Example of Calculation of QFP Fine-Pitch Mounting Pad Dimensions

Unit: mm

Package		Body width E	Body length D	No. of pins/side		Pin pitch e	Mounting width		Pad width b_2	Pad length l_2
No. of pins	Code No.			n_E	n_D		M_{IE}	M_{ID}		
48	S48GA-50-2E5-1	7		12		0.5	6.8		0.25	1.4
	S48GA-50-9EU-1									
64	S64GB-50-9EU-1	10		16			9.8			
72	S72GB-50-2EP-2			18						
80	P80GK-50-BE9-4	12		20			11.8			
	S80GK-50-9EU									
88	S88GK-50-3EQ-1			22						
100	P100GC-50-7EA-2	14		25			13.8			
	S100GC-50-8EU									
	S100GC-50-9EU-1									
120	S120GJ-50-3EB-2	20		30			19.8			
144	S144GJ-50-3EN-2			36						
	S144GJ-50-8EU-2									
	S144GJ-50-JEU, KEU						19.7			1.5
160	S160GM-50-3ED, JED, KED-2	24		40			23.8			1.4
	S160GM-50-8ED-2									
	S160GM-50-JMD, KMD									
176	S176GM-50-3EU, JEU, KEU-2			44						
	S176GM-50-8EU-2									
208	S208GD-50-5EL-1	28		52			28.2			1.6
	S208GD-50-5ML-2						28.4			1.4
	P208GD-50-LML, MML-2									
	S208GD-50-8EU-2						27.8			
240	P240GN-50-LMU, MMU-1	32		60			32.4			
272	S272GP-50-LMU, MMU-1	36		68			36.4			
304	P304GL-50-NMU, PMU-1	40		76			40.4			
100	S100GK-40-9EV	12		25		0.4	11.8		0.2	
120	S120GC-40-9EV	14		30			13.8			
216	S216GM-40-8EV	24		54			23.8			
256	S256GD-40-LMV, MMV-2	28		64			28.4			
376	S376GL-40-LMV, MMV	40		94			40.4			

Notes 1. The mounting pad dimensions in this table correspond to the packages identified by the dimension code No. For the detailed dimensions of each package, refer to the Data Sheet of your product, or “Semiconductor Device Package Manual (C10943X)”.

2. In actual designing, optimization is necessary taking various factors such as mounting density, mountability, and dimensional tolerances into consideration.

(g) Mounting pad of SOJ

The nominal dimensions of an SOJ package are determined by the package width (E).

The center-to-center distance between the mounting pad arrays of an SOJ (e_1) is equal to the distance between the pin arrays, and the pad pitch is equal to the pin pitch e . **Figure 1-11** shows the mounting pad dimensions.

Mounting pad lengths l_1 and l_2 are generally 1.2 mm and 2.0 mm, respectively, for easiness of visual inspection of the solder strength and solderability.

Mounting pad width b_2 is determined by pin width b_1 and pin pitch e .

The mounting pad width of an SOJ is generally 0.76 mm, so that generation of solder bridges is prevented and that visual inspection is easy to conduct.

Figure 1-11. Mounting Pad of SOJ

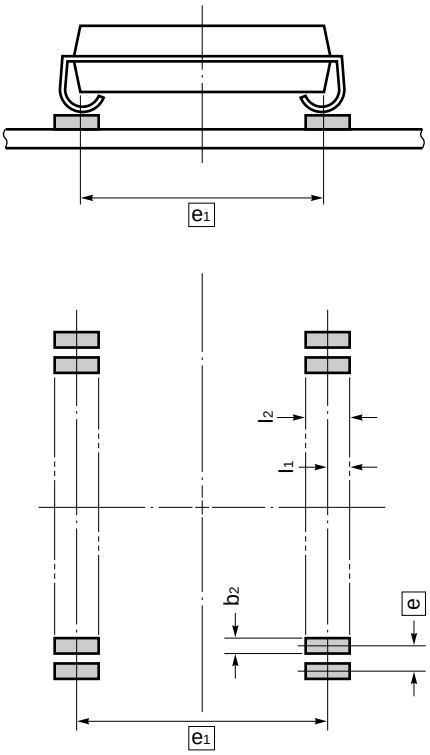


Table 1-6a. Example of Calculation of SOJ Mounting Pad

Unit: mm

Package		Nominal dimension E	Pad width b_2	Pad length		Pin row interval e_1	Pin pitch e
No. of pins	Code No.			l_1	l_2		
24	P24LA-50A-2	7.57 (300 mils)	0.76	1.2	2.0	6.73	1.27
26	P26LA-50A-2						
	S26LA-300A-1						
28	P28LA-300A-1						
32	P32LA-300A-2						
26	P26LA-350A-2	8.89 (350 mils)				8.06	
	P26LB-350A-1						
28	P28LA-400A-2	10.16 (400 mils)				9.40	
	P28LE-400A-1						
	P28LE-400A1						
32	P32LE-400A						
36	P36LE-400A						
40	P40LE-400A-2						
42	P42LE-400A						
44	P44LE-400A						
34	S34LG-500A	12.7 (500 mils)				11.94	

Notes 1. The mounting pad dimensions in this table correspond to the packages identified by the dimension code No. For the detailed dimensions of each package, refer to the Data Sheet of your product, or “Semiconductor Device Package Manual (C10943X)”.

2. In actual designing, optimization is necessary taking various factors such as mounting density, mountability, and dimensional tolerances into consideration.

(h) Mounting pad of QFJ

The nominal dimensions of a QFJ package are determined by package width (E) and package length (D).

Design the mounting pads of this package as follows:

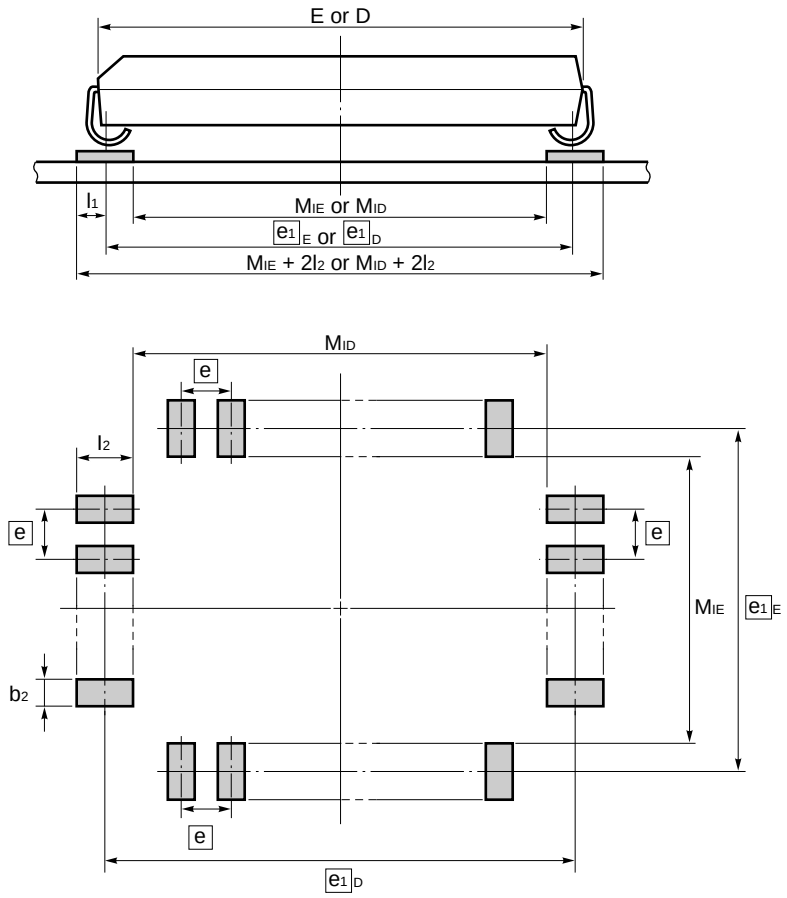
Determine the dimensions of a mounting pad by using the expressions shown in **Figure 1-12**.

Because the width E and length D of the package are known, determine the center-to-center distances between mounting pads $\boxed{e_1}_E$ and $\boxed{e_1}_D$ with the pin row intervals $\boxed{e_1}_E$ and $\boxed{e_1}_D$ based on these parameters. Next, based on these center-to-center distances, determine the lengths of a mount pad l_1 and l_2.

Generally, these lengths are l_1 = 1.2 mm and l_2 = 2.0 mm because visual inspection of solder strength and solderability would otherwise be difficult.

Mounting pad width b_2 is determined by pin width b and pin pitch $\boxed{e}$. The mounting pad width of a QFJ is generally 0.76 mm, so that generation of solder bridges can be prevented and that the solderability can be visually checked with ease.

Figure 1-12. Mounting Pad Dimensions of QFJ (PLCC)



$M_{IE} = \boxed{e_1}_E - 2\,(l_2 - l_1)$

$M_{ID} = \boxed{e_1}_D - 2\,(l_2 - l_1)$

$\boxed{e}$ = 1.27 mm

Table 1-6b. Example of Calculation of QFJ Mounting Pad

Unit: mm

Package		Pad width	Pad length		Pin row interval	Pin row interval	Pin pitch
No. of pins	Code No.	b_2	l_1	l_2	e_1 D	e_1 E	e
18	P18L-50A-2	0.76	1.2	2.0	11.68	6.60	1.27
28	P28L-50A1-2				10.42	10.42	
32	P32L-50A-2				12.95	10.42	
44	P44L-50A1-2				15.50	15.50	
52	P52L-50A1-2				18.04	18.04	
68	P68L-50A1-2				23.12	23.12	
84	P84L-50A3-2				28.20	28.20	

Notes 1. The mounting pad dimensions in this table correspond to the packages identified by the dimension code No. For the detailed dimensions of each package, refer to the Data Sheet of your product, or “Semiconductor Device Package Manual (C10943X)”.

2. In actual designing, optimization is necessary taking various factors such as mounting density, mountability, and dimensional tolerances into consideration.

(i) Mounting pad of plastic BGA

The drawings of cavity up-type mounting pads are shown in **Figure 1-13**, followed by **Table 1-7** which provides detailed information on these pads. Those for cavity-down type pads are provided in **Figure 1-14** and **Table 1-8**.

Figure 1-13. Mounting Pad Dimensions of Plastic BGA (Cavity-Up)

Table 1-7. Example of Calculation of Plastic BGA Mounting Pad Dimensions (Cavity-Up)

Unit: mm

Package		Body width E	Body length D	No. of pins/side		Pin pitch e	Pad layout	Pad diameter ϕb
No. of pins	Code No.			n_E	n_D			
119	P119S1-R4	14	22	7	17	1.27	Full matrix	0.6 ± 0.1
225	P225S1-B1-1	27		15		1.50		
	S225S1-B1-1							
	Y225S1-B1							
256	S256S1-B6-1			20		1.27	Perimeter 4 row	
	Y256S1-B6							
313	S313S1-F5-1	35		13		2.54	Staggered matrix	
	Y313S1-F5							
352	S352S1-F6-1			26		1.27	Perimeter 4 row	
	P352S1-F6			20				
	Y352S1-F6							
396	P396S1-F1					1.50	Full matrix	
	P396S1-F11							

Notes 1. The mounting pad dimensions in this table correspond to the packages identified by the dimension code No. For the detailed dimensions of each package, refer to the Data Sheet of your product, or “Semiconductor Device Package Manual (C10943X)”.

2. In actual designing, optimization is necessary taking various factors such as mounting density, mountability, and dimensional tolerances into consideration.

Figure 1-14. Mounting Pad Dimensions of Plastic BGA (Cavity-Down)

Table 1-8. Example of Calculation of Plastic BGA Mounting Pad Dimensions (Cavity-Down)

Unit: mm

Package		Body width E	Body length D	No. of pins/side		Pin pitch e	Pad layout	Pad diameter ϕb
No. of pins	Code No.			n_E	n_D			
272	S272S2-C6-1	29		21		1.27	Perimeter 4 row	0.6 ± 0.1
416	S416S2-H6	40		30			Perimeter 4 row	
480	S480S2-K6-1	45		34			Perimeter 4 row	
580	S580S2-K6						Perimeter 5 row	
672	S672S2-K6-1						Perimeter 6 row	

Notes 1. The mounting pad dimensions in this table correspond to the packages identified by the dimension code No. For the detailed dimensions of each package, refer to the Data Sheet of your product, or “Semiconductor Device Package Manual (C10943X)”.

2. In actual designing, optimization is necessary taking various factors such as mounting density, mountability, and dimensional tolerances into consideration.

(j) Mounting pad of tape BGA

The drawings of tape BGA mounting pads are shown in **Figure 1-15**, followed by **Table 1-9,** which provides detailed information of these pads.

Figure 1-15. Mounting Pad Dimensions of Tape BGA

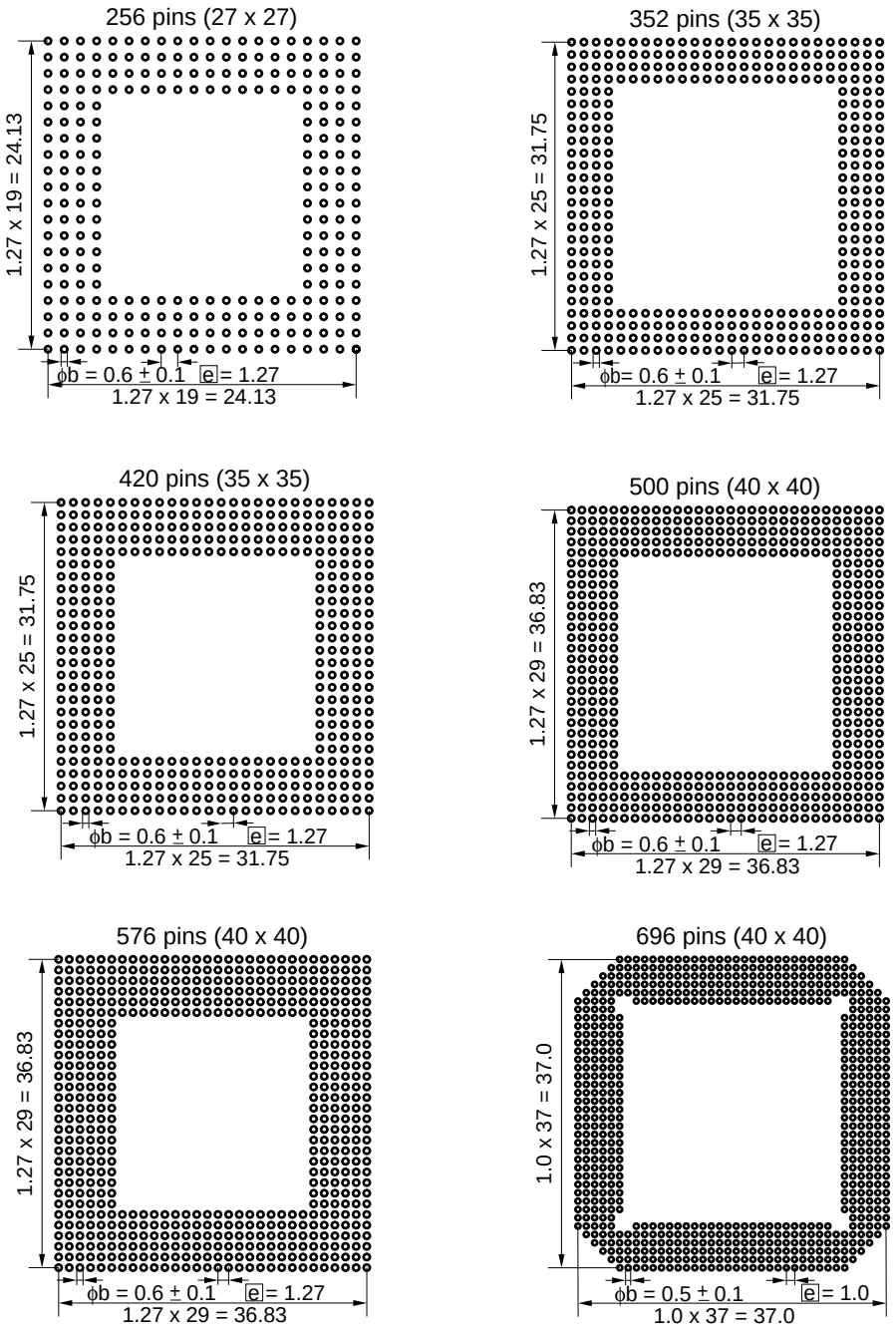


Table 1-9. Example of Calculation of Tape BGA Mounting Pad Dimensions

Unit: mm

Package		Body width E	Body length D	No. of pins/side		Pin pitch e	Pad layout	Pad diameter ϕb
No. of pins	Code No.			n_E	n_D			
256	P256N2-B6	27		20		1.27	Perimeter 4 row	0.6 ± 0.1
	S256N7-B6							
352	P352N2-F6	35		26				
	S352N7-F6							
420	P420N2-F6						Perimeter 5 row	
	S420N7-F6							
500	S500N7-H6	40		30				
576	S576N7-H6						Perimeter 6 row	
696	S696N7-H9			38		1.0		0.5 ± 0.1

Notes 1. The mounting pad dimensions in this table correspond to the packages identified by the dimension code No. For the detailed dimensions of each package, refer to the Data Sheet of your product, or "Semiconductor Device Package Manual (C10943X)".

2. In actual designing, optimization is necessary taking various factors such as mounting density, mountability, and dimensional tolerances into consideration.

(k) Mounting pad of fine-pitch BGA

The drawings of fine-pitch BGA mounting pads are shown in **Figure 1-16**, followed by **Table 1-10**, which provides detailed information of these pads.

Figure 1-16. Mounting Pad Dimensions of Fine-pitch BGA

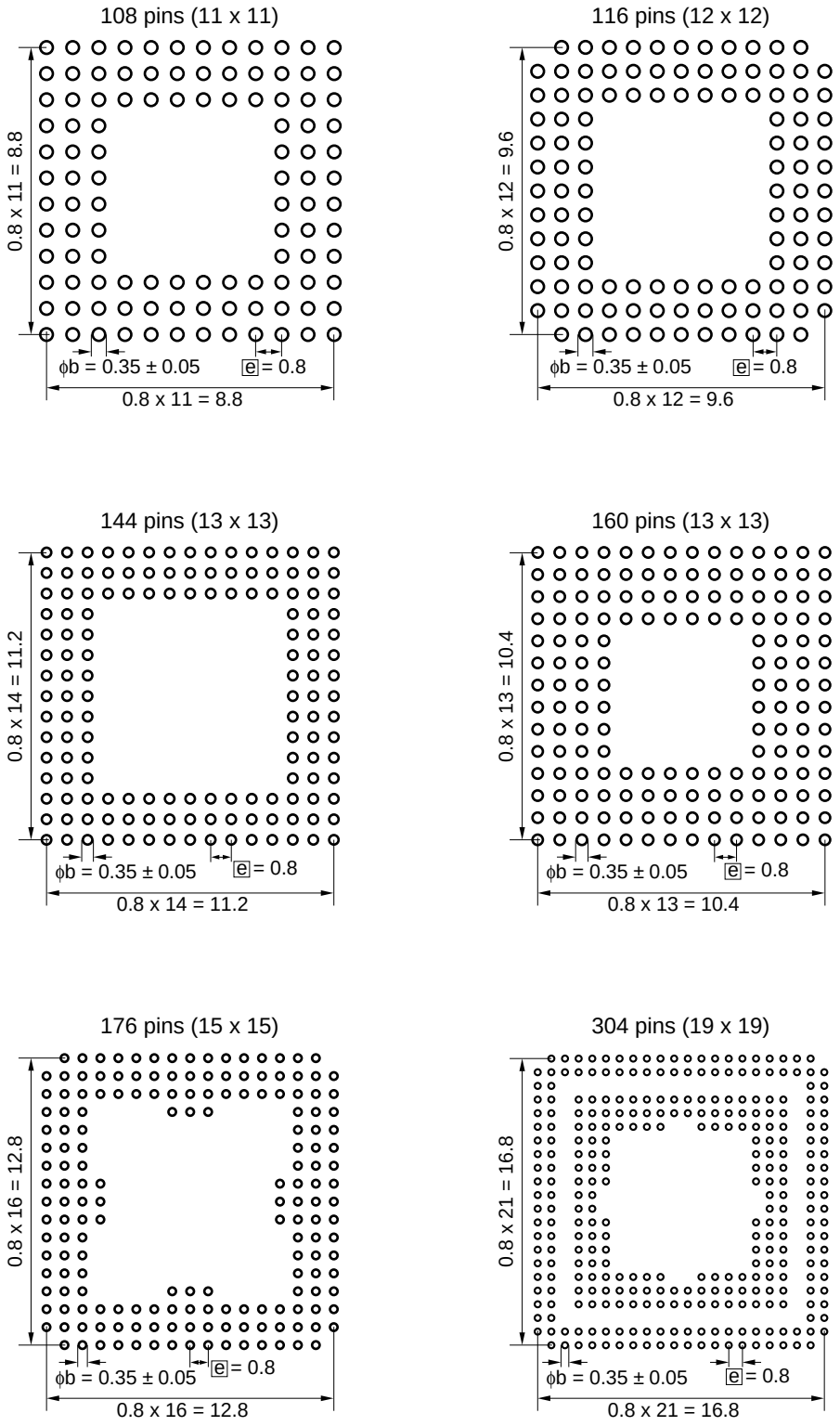


Table 1-10. Example of Calculation of Fine-pitch BGA Mounting Pad Dimensions

Unit: mm

No. of pins	Body width	Body length	No. of pins/side		Pin pitch	Pad layout	Pad diameter
	E	D	ne	ND	e		ϕb
108	11		12		0.8	Perimeter 3 row	0.35 ± 0.05
116	12		13			Perimeter 3 row	
144	13		15			Perimeter 3 row	
160	13		14			Perimeter 4 row	
176	15		17			Perimeter 3 row	
304	19		22			Perimeter 6 row, no 3rd row	

(l) Mounting pad of discrete package

Figures 1-17 through **1-24** show examples of dimensions of the mounting pads of discrete packages.

Figure 1-17. Small E-Mold Package (unit: mm)
(Small ESVAC Mold)

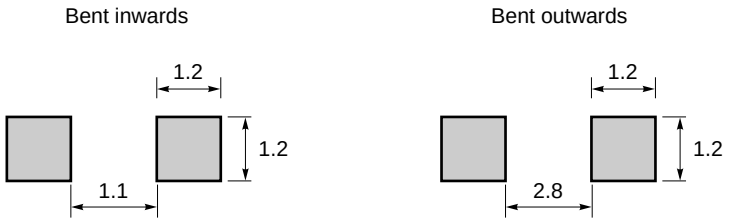


Figure 1-18. Super Small Mini-Mold Package (unit: mm)

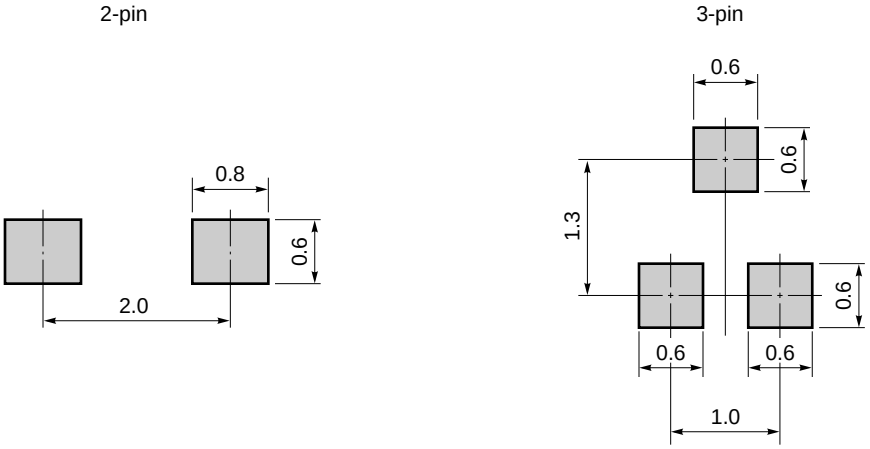


Figure 1-19. Small Mini-Mold Package (unit: mm)

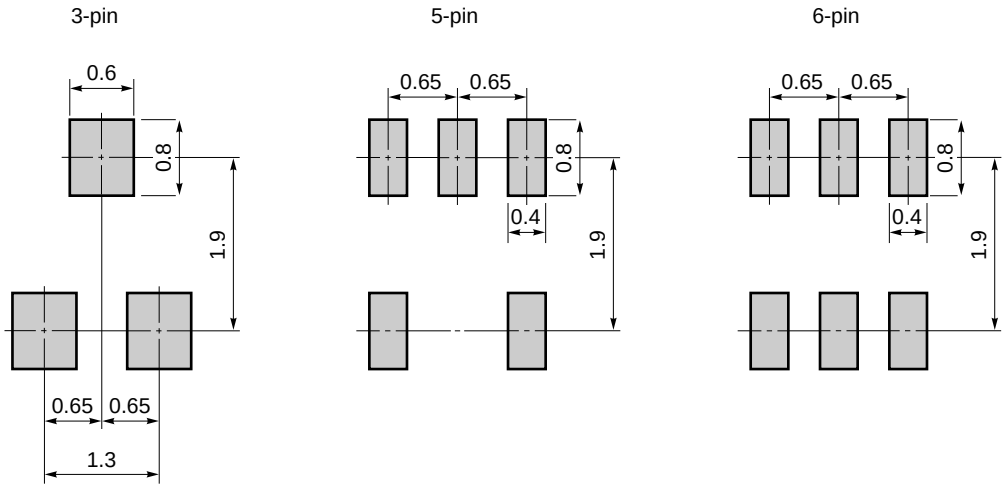


Figure 1-20. Mini-Mold Package (unit: mm)

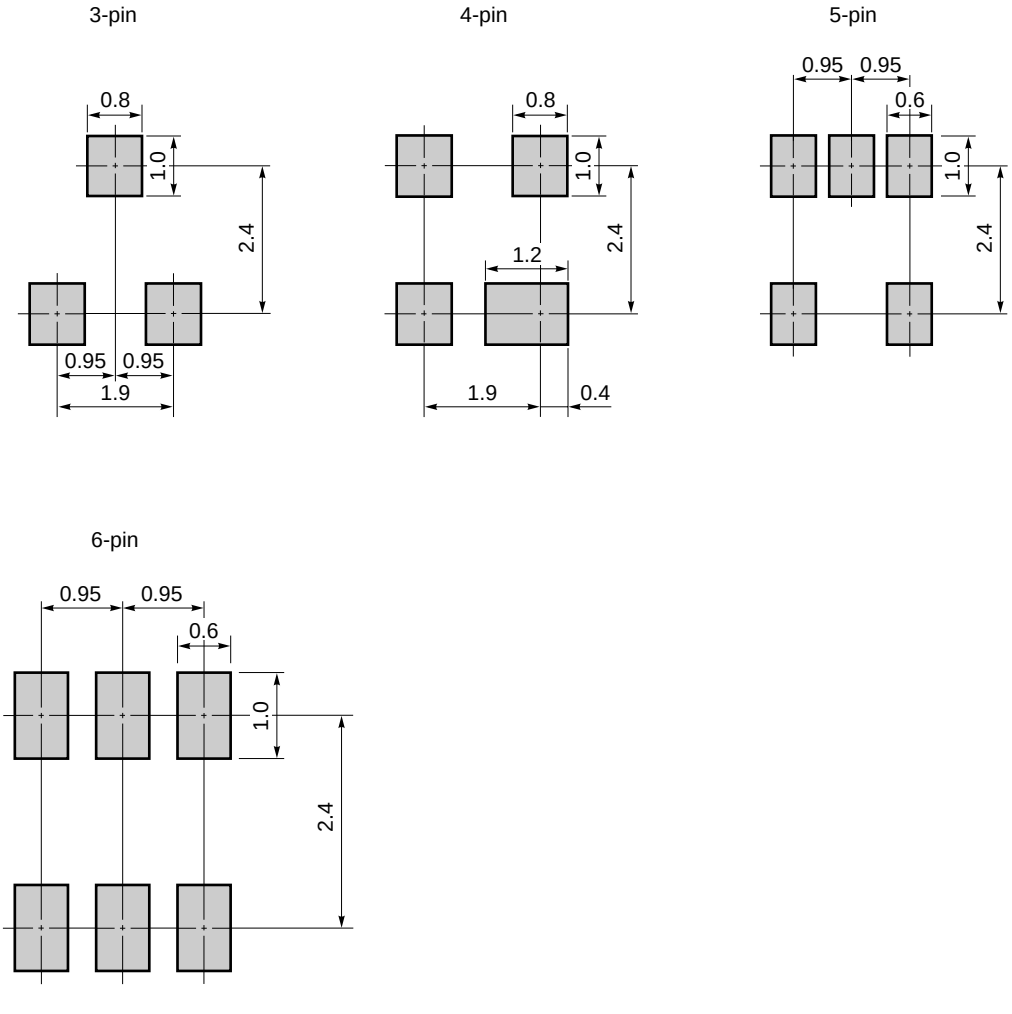


Figure 1-21. Power Mini-Mold Package (unit: mm)

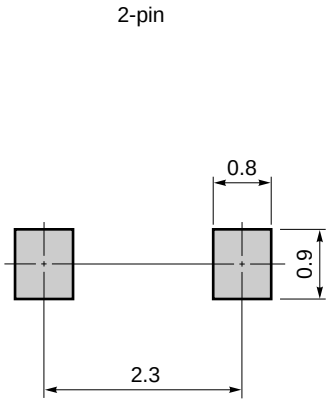


Figure 1-22. MP-2 Package (unit: mm)

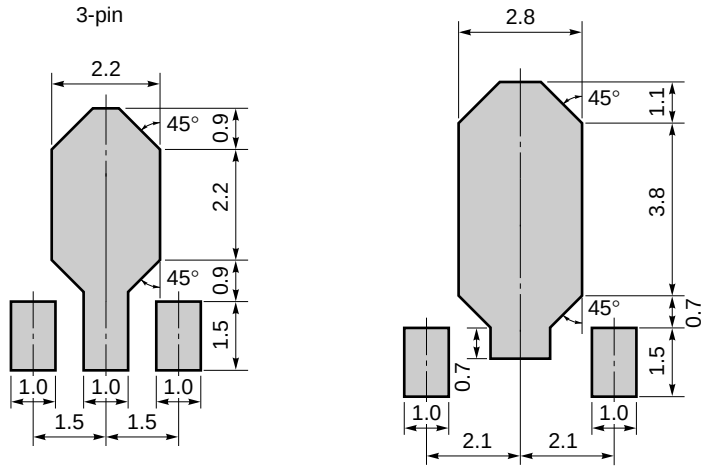


Figure 1-23. MP-3Z Package (unit: mm)

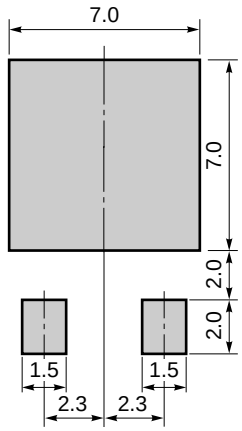
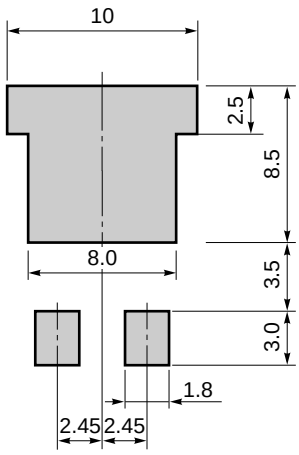


Figure 1-24. MP25-Z Package (unit: mm)



1.2.3 Solder paste and supply method

(1) Solder paste

Solder paste is made of evenly mixed solder powder, flux, and binder agent. Generally, the solder powder uses a composition ratio of Sn60 to 63 or Pb40 to 37. The powder may be ball-shaped or may not have a particular shape at all.

A solder composition ratio must be selected according to the surface material of the pins of the component (i.e., SMD) to be mounted. If the surface material of the pin or conductive electrodes of the PWB is Ag, add several % of Ag to prevent corrosion of the electrodes.

Tables 1-11 and **1-12** list the major solder pastes and their features.

What type of solder paste is used has significant influences on printability and solderability. Therefore, select the solder manufacturer, composition, particle, flux content, and flux component according to your mounting processes.

Table 1-11. Type of Solder Paste

(i) Type of solder paste

Composition	Melting temperature	Particle, mesh	Shape	Flux		Viscosity 10^4 cps	Remarks
				Content	Chlorine content		
Sn63/Pb37	183°C	150 to 400	Non-shaped, ball-shaped	8 to 20 wt%	0.2 wt%	10 to 60	
Sn62/Pb36/Ag2	179°C						Used as Ag electrode

(ii) Type of solder paste (by usage)

Usage	Solder shape	Viscosity 10^4 cps	Solder particle, mesh
Dispenser	Ball-shaped	10 to 30	250 to 400 / 325 to 400
Mesh screen	Ball-shaped	40 to 60	250 to 325 / 325 to 400
Metal screen (film thickness < 1 mm)	Ball-shaped/non-shaped	50 to 80	200 to 325

Table 1-12. Features of Solder Paste (powder)

Compared with:	Non-shaped	Ball-shaped
Viscosity	Good	Poor
Resilience	Poor	Good
Printing method	Suitable for metal mask printing. Suitable for relatively coarse mesh screen	Suitable for relatively fine mesh screen. Metal screen printing can also be used. Suitable for fine pitch pattern
Dispensing	Not so suitable	Suitable

(2) Supply method

The solder paste is supplied by means of screen printing or dispensing. How the solder paste is to be supplied should be determined according to the dimensions of the SMD to be soldered and the characteristics of the solder paste to be used.

The following paragraphs briefly describe how screen printing and dispensing are implemented:

(a) Screen printing

Figure 1-25 illustrates each step of screen printing.

An adequate quantity of the solder paste is supplied on the screen which is pressed against the PWB, onto which the solder paste is to be printed, and moved with a squeegee. The thickness of the solder paste printed on the PWB is almost equal to the thickness of the screen. The quantity of the solder paste to be printed can be calculated by the expression shown in **Figure 1-25**.

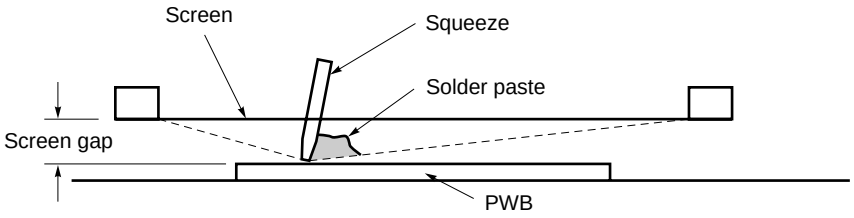
The screen may be of metal or mesh. The metal screen excels in terms of printing accuracy and durability, and is desirable to print the solder paste to solder small, thin packages with many pins.

As the screens for fine pitch patterns, those of materials such as phosphor bronze and metal created by additive method are now available in addition to the existing stainless screen. Consult screen manufacturers for details.

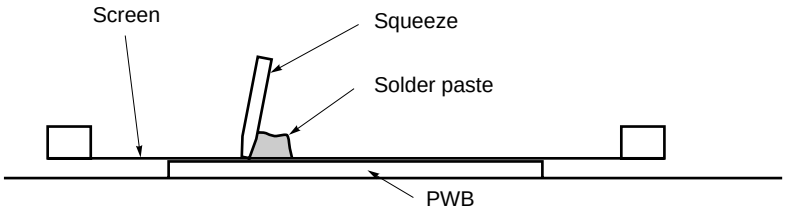
Figure 1-25. Outline of Screen Printing (courtesy: catalog by Senju Kinzoku)

Screen printing

(i) With mesh screen ····· Screen is lifted about 0.3 mm from PWB



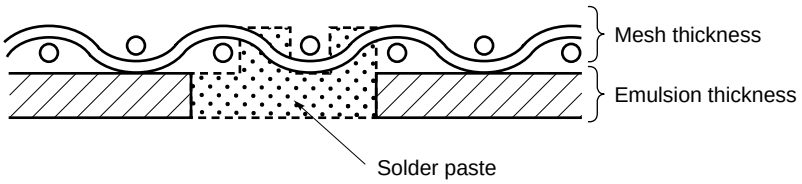
(ii) With metal screen ... Screen is directly placed on PWB



Calculation of quantity of solder paste printed

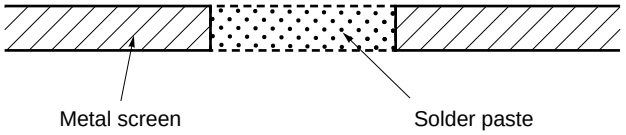
(i) With mesh screen

Quantity of solder paste printed = (Mesh thickness × Space + Emulsion thickness) × Pattern area



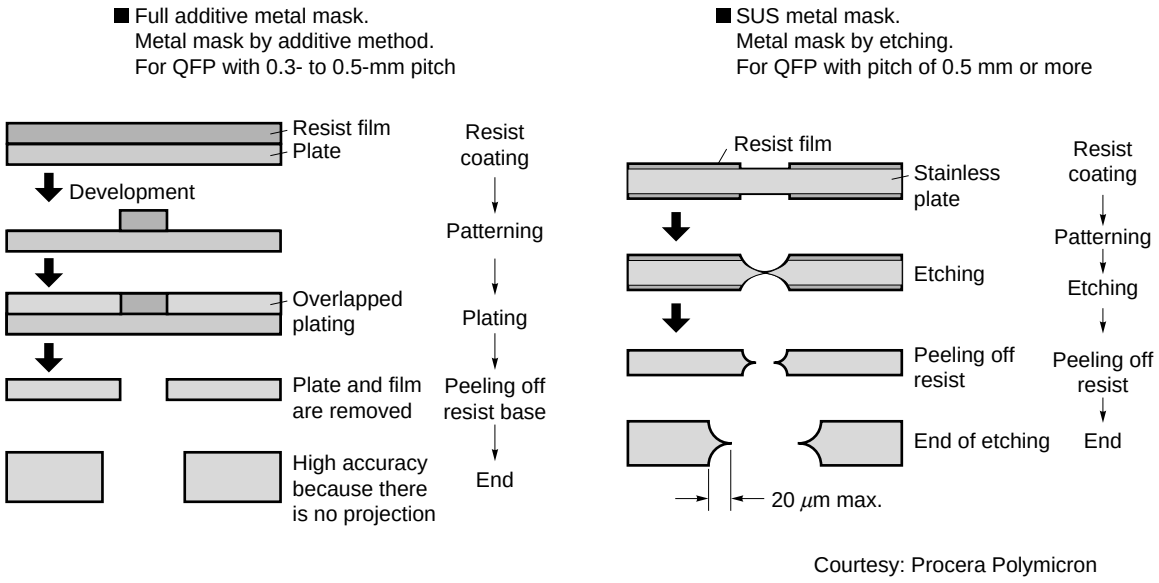
(ii) With metal screen

Quantity of solder paste printed = Screen thickness × Pattern area



The additive method is electro forming method. **Figure 1-26** shows the flow of the conventional SUS metal mask and an additive metal mask created by the additive method.

Figure 1-26. SUS Metal Mask and Additive Mask



Courtesy: Procera Polymicron

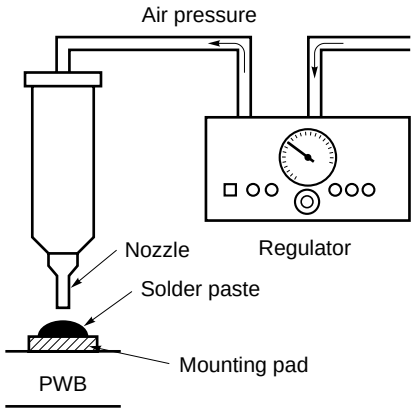
(b) Dispensing

This is a technique to supply a fixed quantity of solder paste onto a PWB by using a dispenser. This method is difficult in controlling the quantity of the supplied solder paste (especially, when supplying the solder paste in small amount), and therefore is used to solder packages with a relatively wide pin pitch (SOPs and QFPs with a pin pitch of 0.8 mm or more).

This method is not recommended to solder packages with a fine pin pitch (less than 0.8 mm) because solder bridges are likely to occur.

Figure 1-27 illustrates how the solder paste is dispensed.

Figure 1-27. Supplying Solder Paste by Dispenser



1.2.4 Adhesive application

Adhesive is used if the SMD cannot be temporarily fixed on a PWB with the solder paste because of insufficient viscosity, or if the SMD is to be soldered by means of reflow soldering.

Two types of adhesives are available: heat-curable and UV-curable adhesive. In general, both the types are used in combination.

To select adhesive, the following points must be noted:

(1) Select an adhesive having enough adhesive strength.

(a) **Figure 1-28** shows a method to evaluate the adhesive strength. **Figure 1-29** shows the result of the evaluation. As shown in this figure, JU-11T or JU-17T (manufacturer: Sanei Kagaku, Distributor: Koki) has the best adhesive strength of the three samples evaluated.
In contrast, the acryl-based adhesive has a poor strength.

(b) The adhesive strength is dependent on temperature. This means that the strength may be degraded while the component (SMD) is soldered, resulting in accidental removal of the SMD from the PWB. Therefore, the dependency of the adhesive strength on temperature must be confirmed in advance. **Figure 1-30** shows an example of changes in adhesive strength with temperature (because the surface condition of the package is different from one SMD to another, the adhesive strength may also vary).

(2) Keep the heating temperature as low as possible, and adhere the SMD in a short time (it is recommended that the adhesive be cured at low temperature and in a short time to maintain the reliability).

Figure 1-28. Evaluating Adhesive Strength

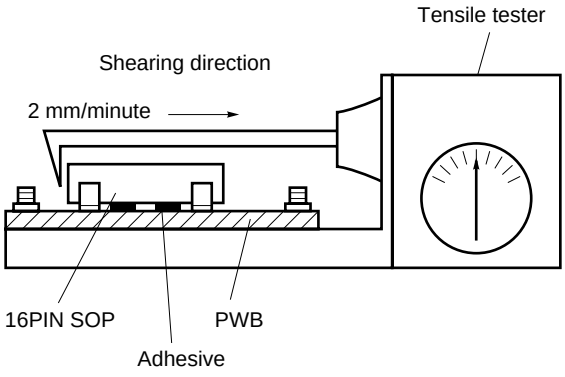
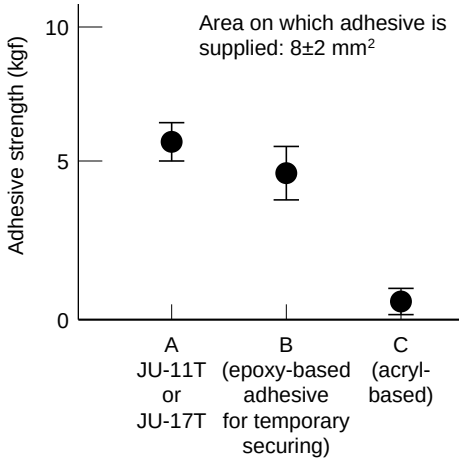


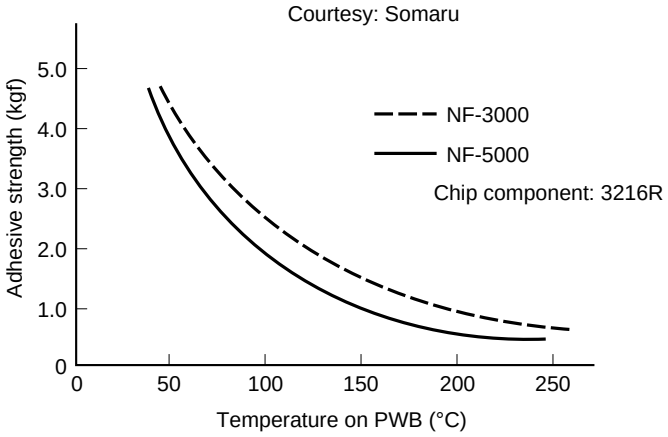
Figure 1-29. Result of Evaluation of Adhesive Strength



= Evaluating adhesive strength =

The adhesive was supplied on the PWB, onto which the SMD was mounted. The shearing strength was then measured with a tensile tester. (The curing conditions recommended by each adhesive manufacturer were satisfied.)

Figure 1-30. Changes in Adhesive Strength with Temperature



The adhesive strength drops once when the temperature rises, but can be restored if the temperature later falls to room temperature.

(3) Determine the quantity of the adhesive to be supplied in accordance with the standoff dimensions and weight of the SMD to be soldered, to prevent ineffective adhesion and soldering.
It is desirable that the curing temperature be less than the glass transfer point (around 150°C) of the plastic package to maintain the SMD's reliability, and be less than the storage temperature specified in each SMD. **Table 1-13** shows the curing conditions of the general adhesives.

Table 1-13. Curing Conditions of Adhesives

Adhesive	Material	Valid period	Curing condition
Heat-curable	Epoxy	1 to 3 months (25°C)	120°C, 90 seconds
UV-curable	Acryl	1 month (25°C)	Exposure to UV (80 W/cm^2), 150°C, 60 seconds
Combination of heat- and UV-curable adhesives	Epoxy	1 to 3 months (25°C)	With UV- and heat-curable: Exposure to UV (80 W/cm^2), 150°C, 60 seconds

For details, consult each adhesive manufacturer.

1.2.5 Placement

Onto the PWB to which the solder paste has been supplied, SMDs are placed semi-automatically or automatically by chip mounting machines.

To transport SMDs to the PWB, the following methods are used:

- Vacuum suction
- Chuck

To place the SMDs onto the PWB automatically, these methods are used:

- Multiple placement
- In-line placement
- One-by-one placement

Each of these placement methods has its own features and must be selected according to the SMD to be placed and mounted onto the PWB.

The SMD package diversifies because:

- Many types of packages are available (e.g., TSOP, fine-pitch QFP, surface mount PGA, BGA, etc.)
- Trend toward finer pitch (e.g., pitch of as fine as 0.5 mm or 0.4 mm)
- Trend toward smaller pins (e.g., total length of fine-pitch QFP: L_1: 1 mm)

[NEC's service regarding placement technology]

(a) Package samples (package not containing chip) are readily available from NEC so that you can confirm the accuracy of your mounting machine when it mounts NEC's SMDs. For details, consult NEC.

(b) NEC's SMDs are available in various packing styles such as magazine case, tray, adhesive taping, and embossed taping, upon your request.

The adhesive taping is low-cost, but the adhesive strength significantly varies and the SMDs may come off the tape if the adhesive strength of the tape is insufficient.

NEC therefore recommends that the embossed taping, which does not have these problems, be used.

Note that the packing dimensions of taping, except the taping standardized by EIAJ and JIS, vary depending on the manufacturers. Consult the manufacturer in advance to confirm that the dimensions match your mounting machines.

1.2.6 Soldering method

(1) Features of soldering method (outline)

The soldering methods can be broadly classified into the partial heating method by which the pins of a package are locally heated, and the whole heating method by which the entire package is heated.

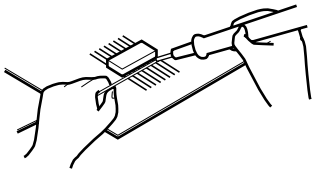
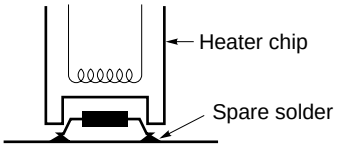
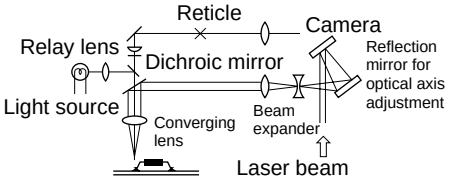
The partial heating method is implemented by using a soldering iron, a pulse heater, laser, light beam, or hot air.

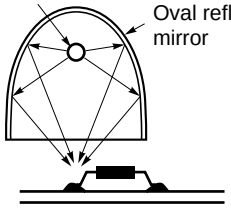
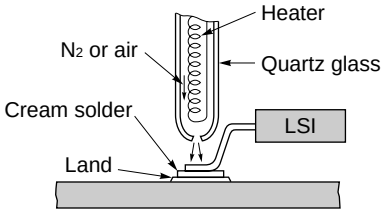
The whole heating method includes infrared reflow, hot air reflow, vapor phase reflow, and wave soldering.

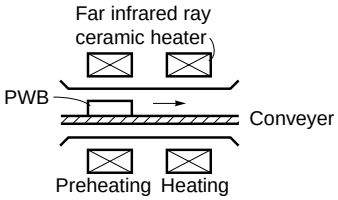
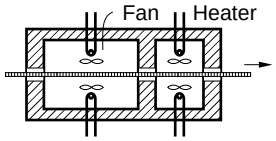
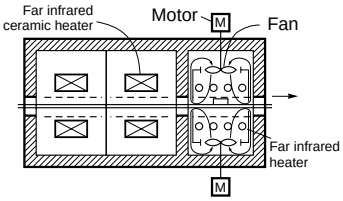
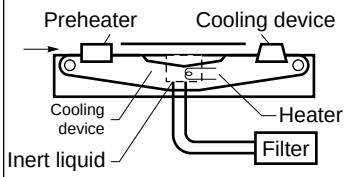
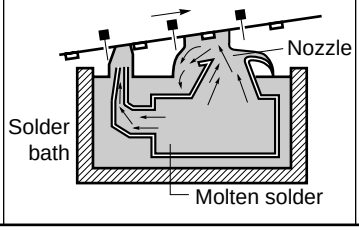
The partial heating method imposes low thermal stress on the PWB, but productivity is poor.

The general heating method is superior in productivity, but imposes a great thermal stress on the components and PWB. **Table 1-14** compares these methods from the viewpoints of thermal stress, running cost, whether each soldering method is applicable to a particular package, and productivity.

Table 1-14. Comparison of Soldering Methods

Division	Simplified name of mounting method	Mounting method	Parameters for comparison			
			Thermal stress on package	Running cost	Restric-tions on applicable packages	Productivity
Partial heating method	Soldering iron heating		Low	High	Exists	Poor
	Pulse heater heating		Low	High	Exists	Poor
	Laser beam heating		Low	High	Exists	Poor

Division	Simplified name of mounting method	Mounting method	Parameters for comparison			
			Thermal stress on package	Running cost	Restric-tions on applicable packages	Productivity
Partial heating method	Light beam		Low	High	Exists	Poor
	Hot air		Low	High	Exists	Poor

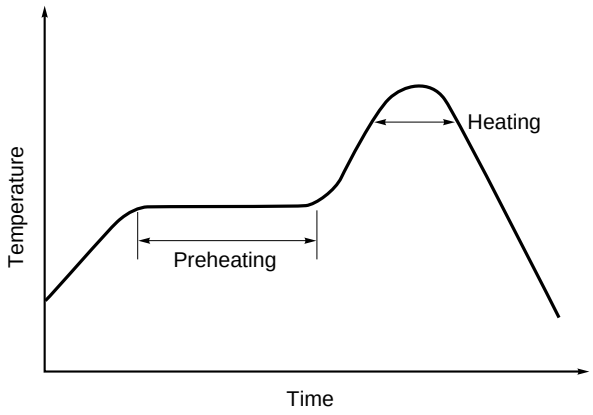
Division	Simplified name of mounting method	Mounting method	Parameters for comparison				
			Thermal stress on package	Temperature variation on package	Running cost	Restrictions on applicable packages	Productivity
Whole heating method	Infrared reflow		High	Large	Low	Exists	Good
	Hot air reflow		Medium	Medium	Low	Does not exist	Good
	Combination of hot air and infrared ray		Medium to high	Medium	Low	Does not exist	Good
	VPS		Medium	Medium	Medium	Does not exist	Good
	Wave soldering		Medium	Small	Low	Exists	Good

(2) Parameters of soldering conditions

Some of the important parameters of the soldering conditions are the temperatures for preheating and heating as shown in **Figure 1-31**.

The following paragraphs describe these parameters in detail:

Figure 1-31. Soldering Temperature Profile



(a) Preheating temperature

Preheating is performed in order to:

- Promote activation of flux
- Prevent abrupt thermal stress
- Preheat PWB (to prevent wicking)

Generally, the preheating temperature is 120 to 150°C.

(b) Heating temperature (for reflow or flow)

The heating temperature is determined by the following factors:

- Melting point of solder paste (eutectic solder: 183°C)
- Resistance to soldering heat of components
- Resistance to soldering heat of PWB

Each soldering method is described in detail next.

Select the soldering method best-suited to your application by giving consideration to the merits and demerits of each method, and resistance to soldering heat of the SMD.

(3) Partial heating method

The partial heating method is mainly used to correct soldering of the SMD that has once been soldered, or to solder an SMD with a poor heat resistance.

When using the partial heating method, observe the soldering conditions recommended by NEC (refer to **Table 1-20** in section **1.4**).

(a) By using soldering iron

A soldering iron is used manually to solder a component after the package of the component has been fixed on a PWB with adhesive.

Determine the wattage of the soldering iron to be used according to the size and shape of the location to be soldered, and the melting point of the solder.

If the soldering temperature is too high, the SMD may be degraded, and the printed wiring of the PWB may be peeled off.

The actual soldering temperature must be determined according to the thermal resistance of the SMD. It is recommended that the temperature characteristics of the SMD be actually measured to determine the soldering temperature. Whenever possible, use a soldering iron whose temperature can be adjusted.

(b) Pulse heater soldering

This method is to melt solder supplied in advance by using joule heat generated by the electric resistance of an electrode or the joint on the PWB to be soldered, and to solder the SMD by applying it a pressure from a heater chip.

This method is not suitable if there is a possibility that the SMD is damaged by leakage current, or to solder packages with J leads such as QFJ and SOJ.

(c) Hot air soldering

This method is to solder the SMD by heating air or N_2 gas with a heater and spraying compressed gas from a nozzle onto the joint on the PWB. The temperature is adjusted by adjusting the heat source or the flow of gas.

(d) Laser soldering

This method is to converge a laser beam into a spot with a lens and cast the beam onto the joint. As the laser, the YAG laser is used.

(e) Light beam soldering

The light emitted from a lamp (xenon lamp) is cast onto an oval reflection mirror to create a certain light flux which is in turn cast onto the joint for soldering.

(4) Whole heating method

The whole heating method generally excels the partial heating method in productivity and running cost and is therefore frequently used.

When using the whole heating method to solder NEC's SMDs, be sure to satisfy the soldering conditions recommended by NEC (refer to **Table 1-20** in section **1.4**).

(a) Infrared reflow soldering

With this method, the SMD is heated by the heat generated from an infrared panel heater or a lamp heater, and soldered onto the PWB.

The infrared ray that is emitted may be the near or far infrared ray. The radiation efficiency of the near infrared ray varies depending on the color and shape of the SMD to be soldered, and especially, is not suitable for soldering SMDs housed in black plastic package because the black package easily cause the temperature to rise. At present, the far infrared ray is mainly used.

The features of infrared reflow soldering are as follows:

(i) Advantages

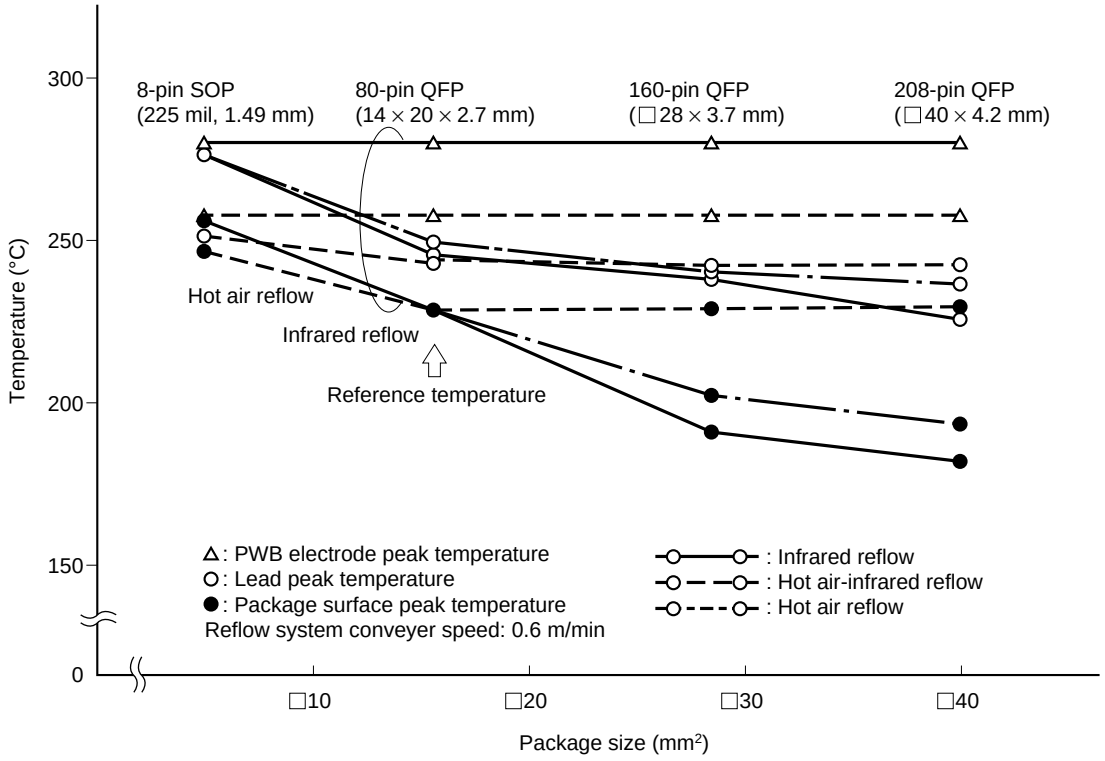
- Low running cost and excellent maintainability
- Short soldering time

(ii) Disadvantages

- Temperature rise on the leads heavily depends on the package size.
  (For an example case, see **Figure 1-32** which shows the relationship between SMD package sizes and peak reflow temperatures.)
- Great thermal stress
- The temperature of the shadowed portion which the infrared ray does not reach does not rise.

Therefore, when various packages exist in mix on the same PWB, or when soldering SOJ and QFJ, determining the appropriate soldering temperature is of vital importance.

Figure 1-32. Correlations between Package Size and Reflow Peak Temperature (comparison of infrared, hot air, and infrared-hot air reflow systems)



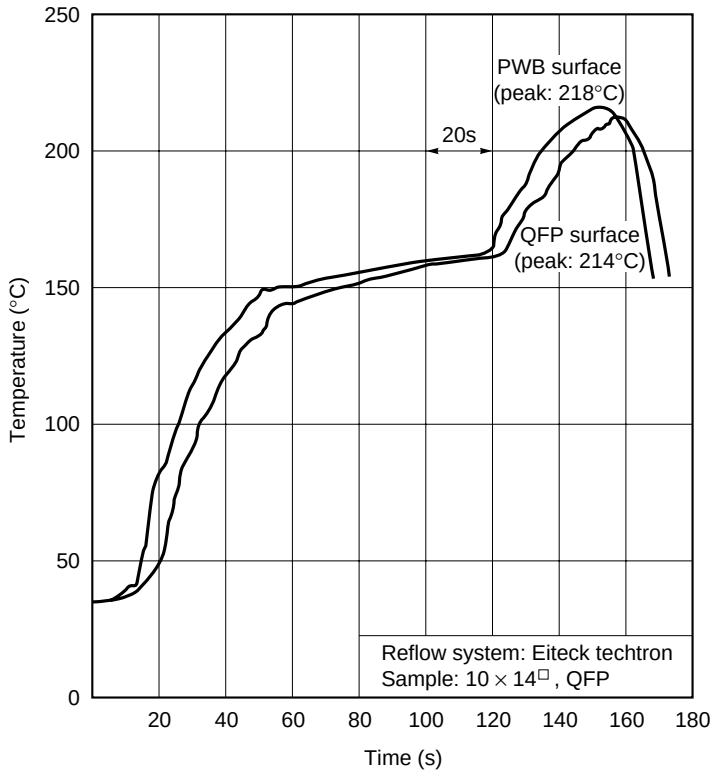
(b) Hot air reflow soldering

Hot air reflow soldering is a method that solves the problems of infrared reflow soldering that the temperatures of the PWB and SMDs on it are uneven. This method also solves the problem of vapor phase soldering (VPS) — high running cost.

The principle of hot air reflow is to heat the SMDs by means of convective heat transfer, i.e., by making air heated by a heater circulate in an oven. Consequently, even if the thermal capacity of the PWB is different from that of the SMDs, the temperature on the PWB and SMDs become uniform after the lapse of a certain time.

Figure 1-33 shows an example of temperature profile of a hot air reflow soldering system.

Figure 1-33. Example of Temperature Profile of Hot Air Reflow Soldering System



The features of hot air reflow soldering are as follows:

(i) Advantages

- Excels infrared reflow soldering in temperature uniformity (temperature is not influenced by the type of SMDs to be heated)
- Relatively low thermal stress

(ii) Disadvantage

- Slightly longer soldering time than infrared reflow

(c) Hot air-infrared reflow

Infrared reflow soldering is used in combination with hot air reflow soldering to shorten the soldering time.

(d) Vapor phase reflow soldering (VPS)

With this soldering method, special inert liquid is heated and boiled with a heater. The SMD to be soldered is subjected to the saturated steam and is soldered by vaporized heat.

As the inert liquid, FC-70 (Sumitomo Three M) and Gulden LS (Nippon Montedison) are used.

The features of VPS are as follows:

(i) Advantages

- Low thermal stress
- Components are evenly heated regardless of their shapes.
- Temperature can be accurately controlled because vaporized heat is used.
- Extremely high heat transfer efficiency makes it possible to lower the heating temperature and shorten the soldering time.
- Little oxidation and dirt on the soldered joint because soldering is performed in inert atmosphere.

(ii) Disadvantages

- High running cost
- Highly toxic parfluoroisobutylen (PFIB) is generated as a result of thermal decomposition of liquid; therefore, a good ventilation system is needed.

When using VPS, the following points must be noted:

- Use inert liquid having a boiling point of 215°C.
- Take adequate countermeasures against tombstone (chip component is lifted from the PWB) and wicking (solder absorbed to pins) phenomena.
  These phenomena are caused because buoyancy is generated as a result of liquefication of vapor and because the temperature on the leads of the SMD rises abruptly and more quickly than the temperature on the PWB. To prevent these phenomena, optimization of the performances of the solder paste, wiring pattern, and temperature rise characteristics of preheating is necessary.
- To obtain stable vapor temperature, the flux to be mixed with the liquid must be sufficiently filtered.

(e) Wave soldering

With this method, molten solder in a soldering bath is ejected to the component on the PWB.
The features of this method are as follows:

(i) Advantages

- Low running cost (SMDs and THDs (through-hole devices) can be soldered at the same time.)
- High productivity (Soldering can be completed in about 5 seconds.)
- Low thermal stress on QFP with high thermal capacity

(ii) Disadvantages

- Difficult to solder various packages (such as fine-pitch package and J-lead package)
- Self-alignment effect cannot be expected (because the components are temporarily fixed on the PWB with adhesive).

(5) Comparison of thermal stress of each method

The partial heating method is ideal for soldering an SMD because the thermal stress is low and therefore, the reliability of the SMD can be maintained. Actually, however, the general heating method is adopted because an emphasis is placed on high productivity.

Each general heating method has its own features, and the thermal stress imposed on the SMD also differs depending on the method.

(a) Comparison of thermal stress of each soldering method

Figure 1-34 shows the influences on the component by infrared reflow, VPS, wave soldering (without preheating), hot air, hot air-infrared reflow, and dip soldering, expressed as relations between heating time and moisture resistance (PCT) (at 125°C, barometric pressure of 2.3, 100% RH).

The heating conditions of each soldering method are as follows:

- Infrared reflow
Hot air reflow
Hot air-infrared reflow ... Peak: 240°C, 210°C min., time variable (package surface temperature)
- VPS ... Peak: 230°C, 200°C min., time variable (package surface temperature)
- Wave soldering ... Solder temperature: 260°C, dipping time variable
- Dip soldering ... Solder temperature: 260°C, dipping time variable

(**Table 1-15** outlines these soldering methods.)

As is evident from **Figure 1-34**, the thermal stress considerably varies depending on the soldering method. Moreover, it can be conjectured that wave soldering and dip soldering are heavily influenced by heating time, but that infrared reflow, hot air-infrared reflow, hot air, and VPS reflow are not much influenced by heating time.

Figure 1-34. Influences on Moisture Proofness by Soldering Conditions

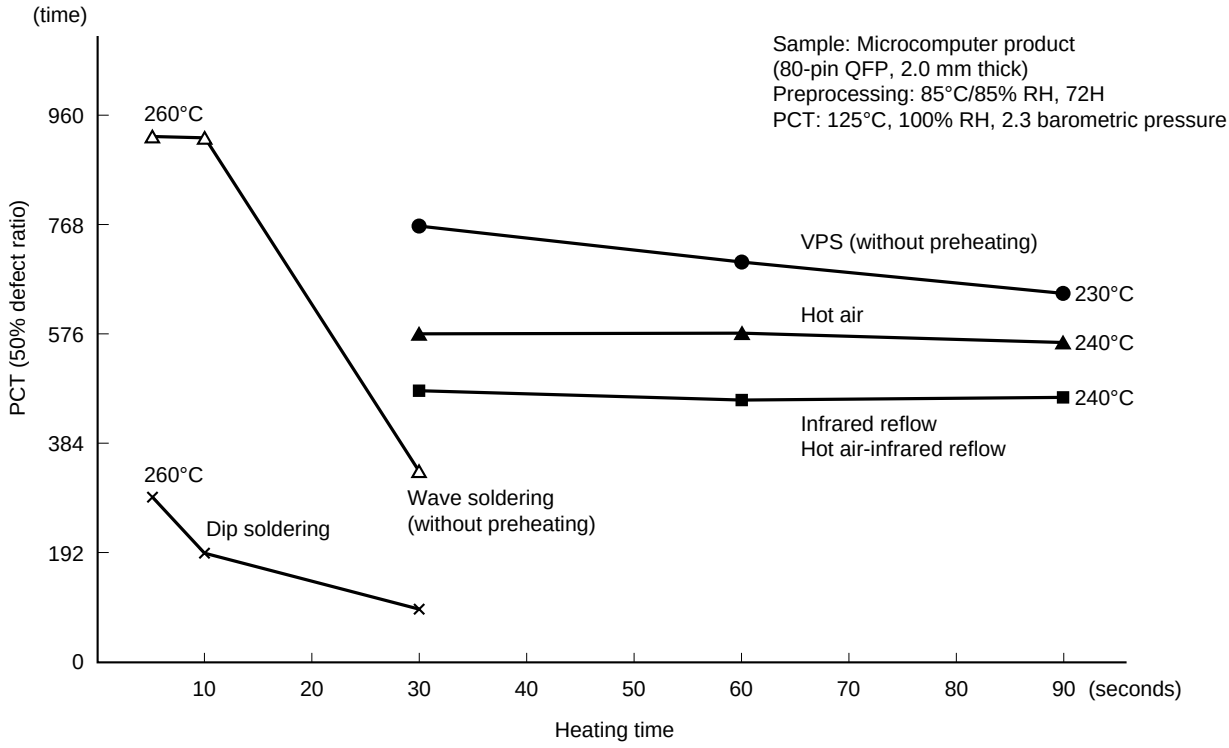
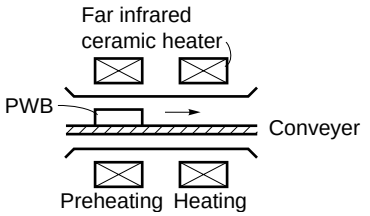
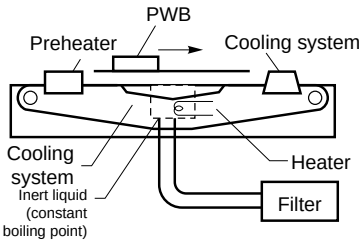
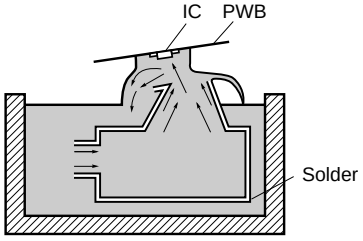
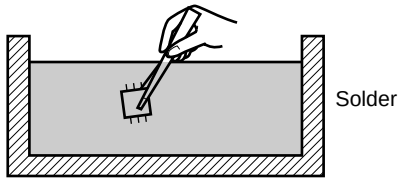
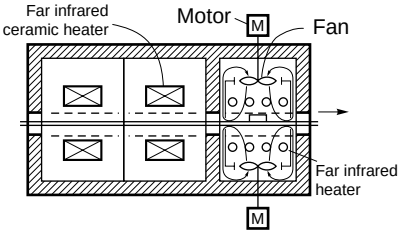
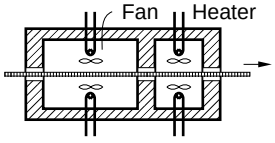


Table 1-15. Outline of Each Soldering Method

Infrared reflow		Vapor phase reflow	
Wave soldering		Dip soldering (for evaluation)	
Hot air-infrared reflow		Hot air	

(b) Relations between internal temperature of package and package cracks

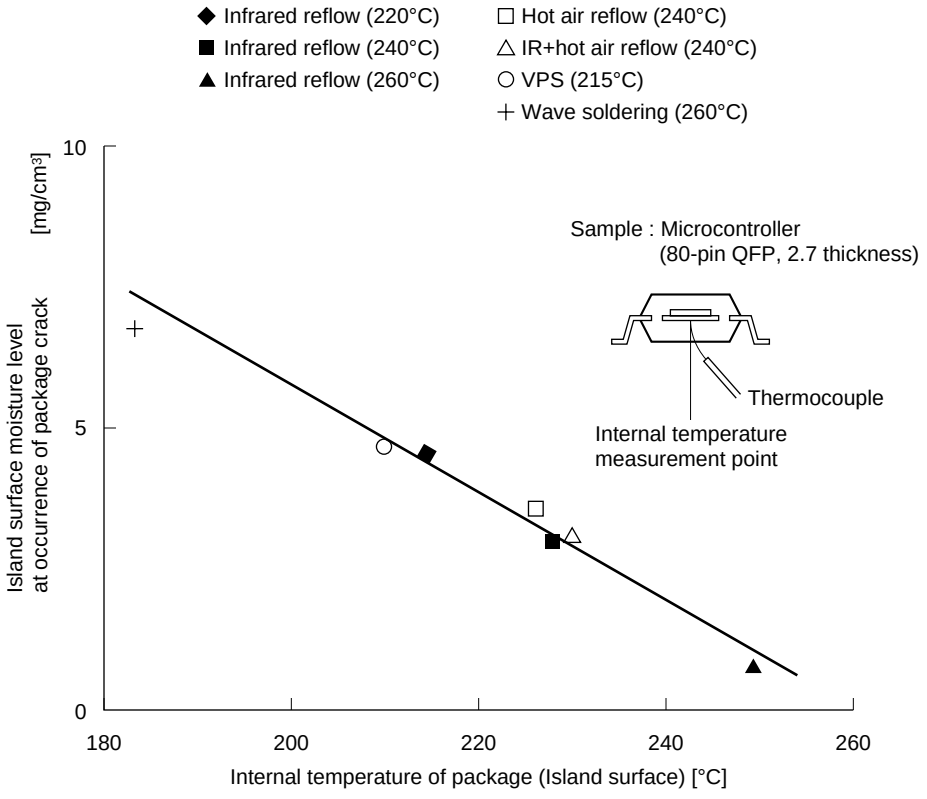
Figure 1-35 shows the relations between the internal temperature of packages and the moisture concentration that causes package cracks, for different soldering conditions.

Infrared reflow	Peak temperature: 220˚C, Time when temperature is higher than 210˚C: 20 secs (Package surface temperature)
	Peak temperature: 240˚C, Time when temperature is higher than 210˚C: 30 secs (Package surface temperature)
	Peak temperature: 260˚C, Time when temperature is higher than 210˚C: 40 secs (Package surface temperature)
	Peak temperature: 240˚C, Time when temperature is higher than 210˚C: 40 secs (Package surface temperature)
Hot air reflow	Peak temperature: 240˚C, Time when temperature is higher than 210˚C: 40 secs (Package surface temperature)
Infrared + hot-air reflow	Peak temperature: 240˚C, Time when temperature is higher than 200˚C: 40 secs (Package surface temperature)
VPS	Peak temperature: 215˚C, Time when temperature is higher than 200˚C: 20 secs (Package surface temperature)
Wave soldering	Solder temperature: 260˚C, Duration: 10 secs, preheating: 120˚C, 4 min

The data above shows that the internal temperature of the package depends on the soldering method that is used, and that the higher the internal temperature, the lower the moisture level when package cracks occur.

Figures 1-34 and **1-35** show general trends, which may not exactly fit all SMDs.

Figure 1-35. Relations between Internal Temperature of Package and Package Cracks



1.2.7 Types of fluxes and cleaning

To solder SMDs, flux is applied to the SMD. After the SMD has been soldered, it is cleaned to eliminate flux residues, solder waste (solder ball), and other impurities.

(1) Types of fluxes

The flux is used for the following purposes:

- To eliminate oxide substances from components and pattern surface
- To prevent re-oxidization during soldering
- To lower the surface tension of molten solder

In other words, the flux is used to improve the solderability.

The fluxes are classified into the following types:

- R type (rosin base)
  Inert rosin flux. Anti-corrosive
- RMA type (mildly activated rosin base)
  Mildly activated rosin flux. Anti-corrosive. Better solderability than R type
- RA type (activated rosin base)
  Strongly activated rosin flux. Better solderability than R and RMA types, but more corrosive

Generally, the R type flux is used, but many types of solder paste contains the RMA type flux.

In general, water-soluble flux contains much chlorine and may affect the reliability of semiconductor devices. Even if the rosin-based flux is used, various substances are contained in the flux residues after soldering, which may cause phenomena such as corrosion of the leads of the package and the conductors on the PWB and insulation degradation at high temperature and humidity.

(2) Cleaning solvent

The cleaning solvent to be used must have the following characteristics:

- Selective solubility: Only dirt such as flux must be solved and the components to be cleaned must not be adversely affected.
- High penetrability: The solvent must be able to enter tiny spaces such as bottom part of the components.
- Low boiling point: The boiling point of the solvent must be sufficiently low so that the components are not subject to thermal stress.
- Stability: When the solvent is decomposed, it must not damage the components or equipment.
- Safety: The solvent must not catch fire or explode.
- Ecological: The solvent must not contaminate the environments.
  (Especially, fleon-based and chlorine-based solvents easily damage and contaminate the environments, and regulations to limit the production and consumption of these solvents have been reinforced in recent years.)

(3) Cleaning methods

Ultrasonic cleaning, immersion cleaning, shower (spray) cleaning, and vapor cleaning are the methods often employed. The following paragraphs outline each of these cleaning methods. Actually, however, these cleaning methods are used in combination for precise cleaning.

- Ultrasonic cleaning
  This method is to apply ultrasonic vibration to the cleaning solvent and is suitable for cleaning of tiny spaces. However, the ultrasonic vibration may damage the components. This method is especially not suitable for cleaning hollow components such as ceramic packages.
- Immersion soldering
  With this method, the component is cleaned dipped in a solvent.
  When using this method, maintenance of the solvent is important because impurities may enter the solvent, causing contamination.
- Shower (spray) cleaning
  This method is to spray the cleaning solvent to the SMD.
- Vapor cleaning
  With this method, the cleaning solvent is vaporized. This method is mainly used for finishing cleaning.

(4) Notes

When cleaning the soldered component, the following points must be noted to maintain the reliability of the SMD:

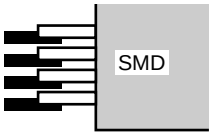
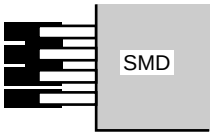
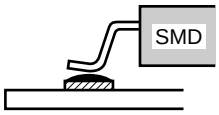
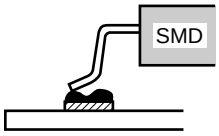
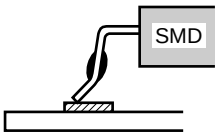
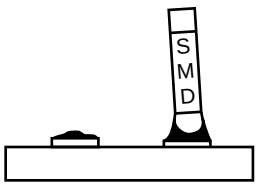
- Cleaning must be carried out at a temperature as low as possible in a short time. Do not touch the cleaned component with your hands until it dries up.
- If the cleaning conditions are not appropriate, the marking on the SMD may be diminished or erased.
- Do not use ultrasonic cleaning to clean hollow packages such as canned case and ceramic.
- Solder waste and impurities may degrade the insulation and characteristics of the SMD. Thoroughly evaluate the PWB on which the SMD is to be soldered to prevent such degradation.

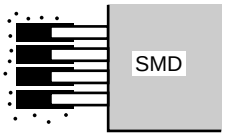
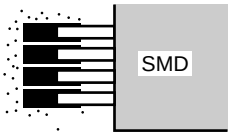
1.2.8 Appearance inspection

The appearance of the soldered joint is mainly inspected visually. In recent years, appearance inspection machines of image recognition type have been increasingly introduced.

Table 1-16 shows the particulars of the inspection.

Table 1-16. Particulars of Appearance Inspection

Item	Outline	Symptom	Cause
Displacement		Relative position of SMD pin and pad is displaced	• Low accuracy of mounting machine • Dimensional tolerance of component unsatisfied • SMD moved by vibration while transported • SMD moved by flux during reflow
Bridge (excessive solder)		Solder remains between adjacent pads or pins	• Too much solder. Solder paste shifted during printing • Bent pin of SMD • Incorrect dimensions of pad and resist. Low accuracy
Pin lifted from PWB surface		Pin lifted from PWB surface and not soldered	• Dimension of flat part of pin (y) of SMD not as specified • Unmatching between above dimension and solder thickness • Low pressure of mounting machine to press component • Pin deformed by contact with other objects while SMD handled
Not enough wetting		Solder not spread enough on pad and pin	• Small quantity of solder paste • Low soldering temperature • Pad and SMD pin not wetted with solder enough (due to oxidization) • Degradation of solder paste
Wicking		Solder absorbed by upper portion of pin and not enough solder left on joint	• Pin temperature rises more quickly than that on pad on PWB to melting point of solder during reflow
Manhattan (tombstone) phenomenon		Chip component stands upright during soldering	• Uneven reflow temperature • Uneven quantity of printed solder • Uneven pad dimension

Item	Outline	Symptom	Cause
Solder ball		Solder ball around pad or SMD	• Displacement or blurr of printed solder paste • Solder paste flowing out to unexpected location due to heating • Ultra minute powder in solder paste not eliminated
Flux residue		Flux residue on surface of PWB after cleaning	• Insufficient cleaning • Incorrect cleaning conditions (cleaning method, solvent, temperature, time)

1.3 Determining Soldering Conditions

The soldering conditions must be determined based on the following factors. Because SMDs are especially designed to be small and thin, their reliability may be degraded if excessive thermal stress is imposed.

<<Factors>>

<1> Resistance to soldering heat

<2> Reliability of soldering (lead wettability)

1.3.1 Resistance to soldering heat

Although small in quantity, a plastic package absorbs moisture even when it is stored at room temperature. If the package absorbing moisture is subjected to thermal stress of soldering, the following problems may arise:

<<Problems>>

<1> The package surface may be expanded or cracked (see **Photo 1-1**).

<2> The reliability of the IC may be degraded.

<3> The chip may be damaged due to aluminum slide, etc.

<4> The bonding wire may break.

This section describes the mechanism and causes of these problems, and countermeasures, and at the same time, the moisture absorption and dry characteristics of plastic packages.

(1) Mechanism of degradation

Figure 1-36 illustrates how a package crack occurs. The following paragraphs describe the outline of each cause of crack occurrence:

(a) Moisture absorption of package

The plastic package is made of epoxy-based mold resin. Because the molecule of this epoxy resin is coarse, the package absorbs a small amount of moisture contained in air if it is stored at room temperature.

Figures 1-37 and **1-38** show examples of the moisture absorption behavior.

Photo 1-1. Cross-Sectional View of Package Crack

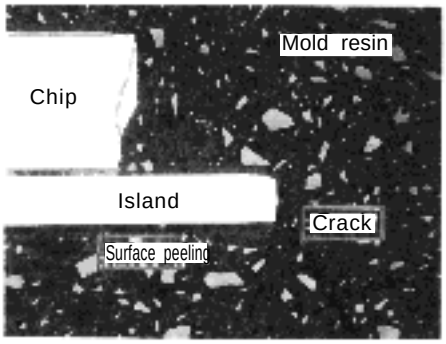
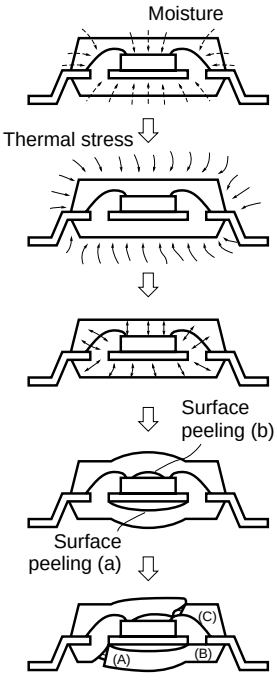


Figure 1-36. Mechanism of Package Crack Occurrence



(i) Moisture absorption of package
- Bulk absorption
- Surface absorption

(ii) Mounting process
- Abrupt thermal stress
- ↓
- Abrupt rise of package temperature

(iii) Increase in internal force of package
- Vaporization and expansion of absorbed moisture
- Difference in thermal expansion of each material

(iv) Occurrence of surface peeling
(→ concentration of internal force)
- Peeling occurrence mode ratio
(a) > (b)

(v) Occurrence of package crack
(→ decrease in internal force)
- Crack occurrence mode ratio
(A) ≒ (B) > (C)

These figures indicate that a thin type SMD absorbs moisture of up to 0.36 wt% when it is stored outdoors, and up to 0.27 wt% when stored indoors (in Tokyo).

The maximum moisture absorption when the sample is stored outdoors is equivalent to a saturated absorption rate at about 30°C, 75% RH, and that when the sample is stored indoors is equivalent to a saturated absorption rate at about 25°C, 65% RH.

The maximum value was observed in summer when the temperature and humidity rise, and the minimum value was recorded in winter when the temperature drops.

Based on these data, NEC specifies, as moisture processing conditions, 30°C, 85% RH for the products for which moisture control is not necessary, and 30°C, 70% RH for the products for which moisture control is necessary (both conditions are determined by taking into consideration areas where temperature and humidity are high).

(b) Mounting process (thermal stress application)

When the package that has absorbed moisture is mounted on a PWB is subjected to an abrupt thermal stress (especially if the package is mounted by means of general heating method), the package temperature rises abruptly.

(c) Increase in internal force of package

When the temperature rises, the moisture absorbed by the package is vaporized and expanded, generating a great stress inside the package. In addition, because the package is heated, the strength of the resin is degraded and unmatching of thermal expansion rate of each constituent elements occurs.

Figure 1-37. Moisture Absorption Behavior of Package (when stored outdoors for 1 year)

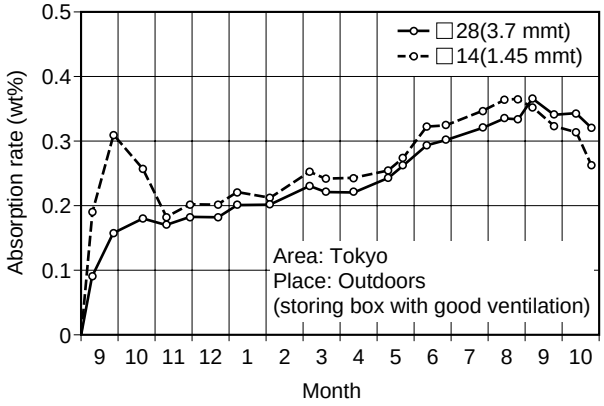
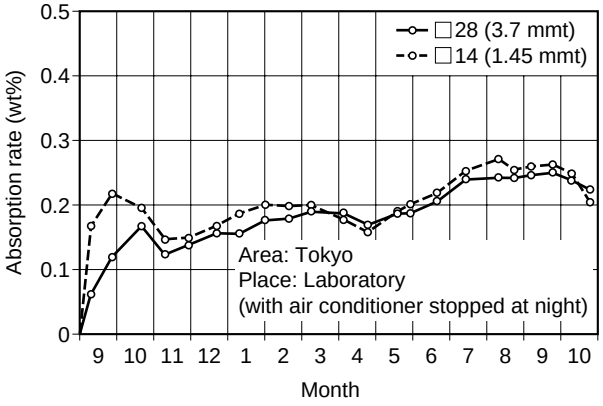
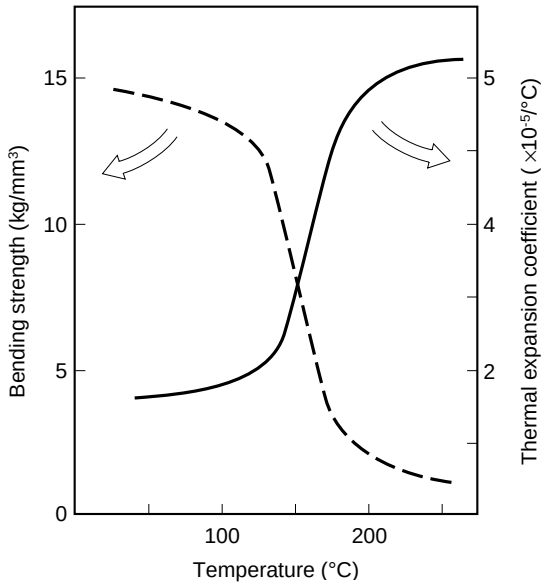


Figure 1-38. Moisture Absorption Behavior of Package (when stored indoors for 1 year)



(**Figure 1-39** shows changes in the characteristics of the resin due to temperature rise. This figure indicates that the thermal expansion coefficient of the resin substantially increases, and the bending strength substantially drops if the temperature rises exceeding the glass transfer temperature.)

Figure 1-39. Dependency of Bending Strength and Thermal Expansion Coefficient of Insulated Resin on Temperature



(d) Occurrence of surface peeling → concentration of internal force

Surface peeling occurs if the stress generated inside the package exceeds the adhesive force of the resin and inserted parts (lead frames and IC chip). This phenomenon most likely occurs on the rear surface of the island which does not so tightly adhere to the resin but occupies the largest area in the package. As a result of peeling, the package may expand and stress is concentrated on the edge part of the peeling.

(e) Occurrence of package crack

The package is cracked if the stress concentrated on the edge of surface peeling exceeds the strength of the resin. If the internal stress generated is too great, or if adhesion between the resin and chip surface is not enough, peeling may also occur on the surface of the chip, or the package may be cracked. This phenomenon may lead to damages to the chip surface or a break of the bonding wires. Peeling of this type causes direct penetration of water or impurities onto the chip surface or corrosion of aluminum wiring (leading to degradation of the moisture resistance of the device).

(2) Causes and influences of degradation

The following factors are causes of package crack (or degradation of moisture resistance):

<<Factors>>

<1> Moisture absorption of package before soldering and mounting

<2> Mounting conditions

<3> Package structure

- Island size
- Package thickness

(a) Moisture absorption of package before soldering and mounting

Figure 1-40 shows the influences of the moisture absorption of the package on the SMD before the device is soldered and mounted.

This figure illustrates the relations between the threshold moisture absorption rate and time when thermal stress of infrared reflow soldering is imposed on the sample.

The threshold moisture absorption rate, beyond which the package is cracked, is 0.18 wt% when the sample is stored at 85°C, 85% RH for 14 hours, and 0.125 wt% when the sample is stored at 30°C, 70% RH for 192 hours.

Figure 1-41 shows a moisture concentration model in the package when a crack occurs. The moisture concentrations on the rear surface of the island (metal plate on which the chip is placed) coincide when the crack has occurred. Therefore, it can be concluded that the package crack is dependent upon the moisture concentration on the rear surface of the island, not upon the moisture absorption rate.

(b) Influence of mounting conditions on device reliability (moisture resistance and crack)

We have already seen the influences of the soldering conditions (soldering method, temperature, and time) on device reliability (moisture resistance and crack) on **Figures 1-34** and **1-35**.

These figures indicated that the reliability of a device is heavily influenced by the soldering method and the heating conditions for soldering.

Figure 1-40. Relations between Occurrence of Package Crack and Moisture Absorption Rate (sample: microcomputer product)

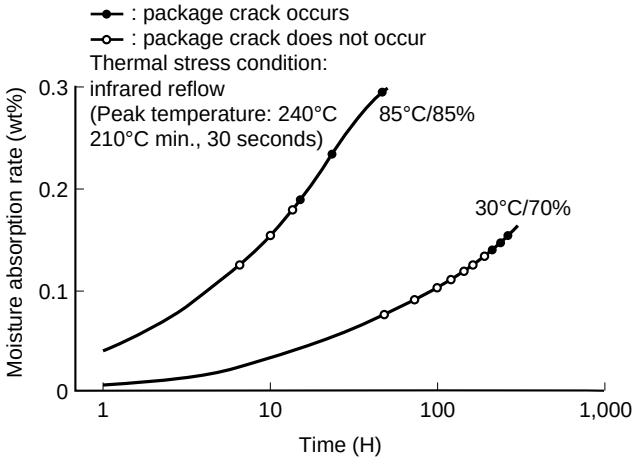
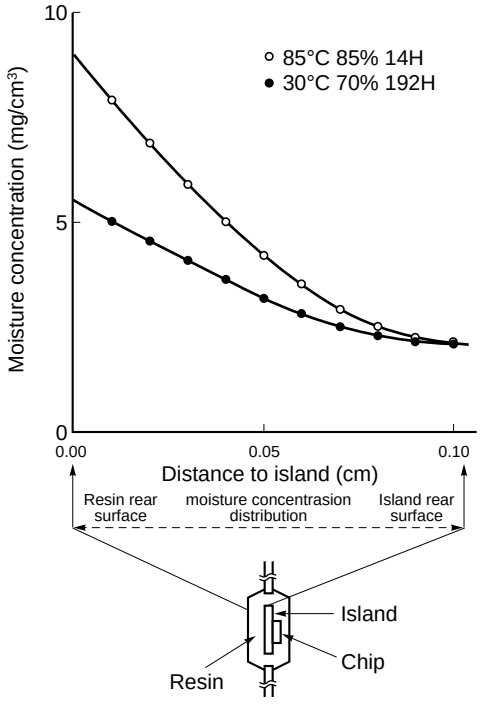


Figure 1-41. Moisture Concentration Characteristics



(c) Package structure

Figures 1-42 and **1-43** show the relations of island size and island back surface moisture concentration at crack occurrence obtained by simulation.

These figures indicate that the package crack tends to occur as the island size becomes larger. **Figure 1-42** shows that the crack tends not to occur as the package becomes thicker. **Figure 1-43** shows that the occurrence of the crack can be suppressed if reflow temperature is lowered even in the case of large island size packages.

Figure 1-42. Relation between Package Thickness and Moisture Concentration

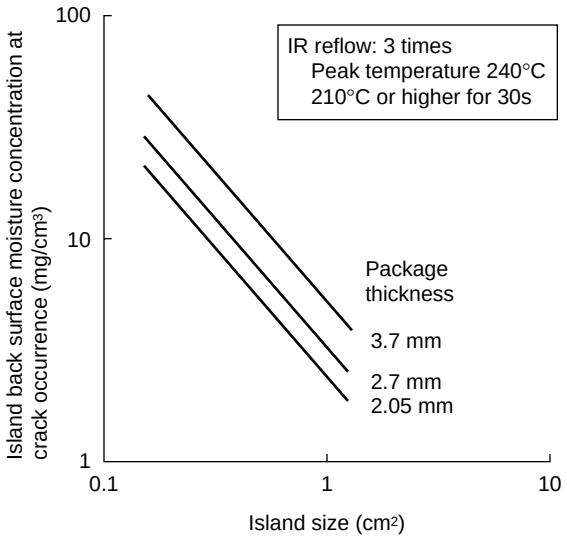
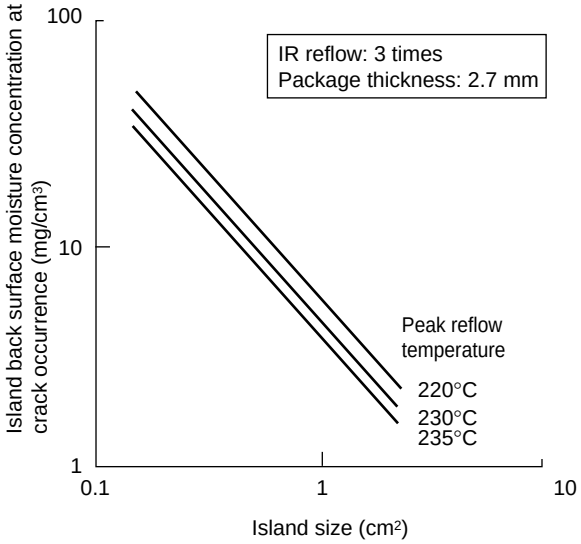


Figure 1-43. Relation between Peak Reflow Temperature and Moisture Concentration



(3) Countermeasures

Figure 1-44 shows the relations among the above causes of package crack and degradation of reliability. This figure indicates that the following countermeasures should be taken to prevent occurrence of package crack and reliability degradation, and to expand the safety region:

<<Points>>

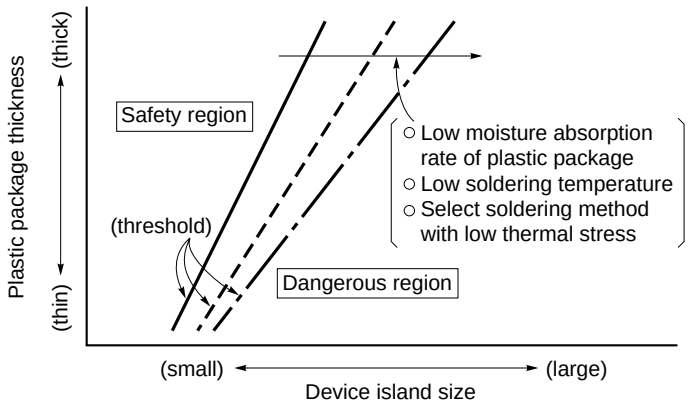
<1> Control must be made so that the moisture absorption rate of the package is lowered.

<2> Select a soldering method with a low thermal stress.

<3> Perform soldering at as low a temperature as possible.

<4> Whenever possible, select a thick package.

Figure 1-44. Influences of Each Cause



(4) Moisture absorption and drying

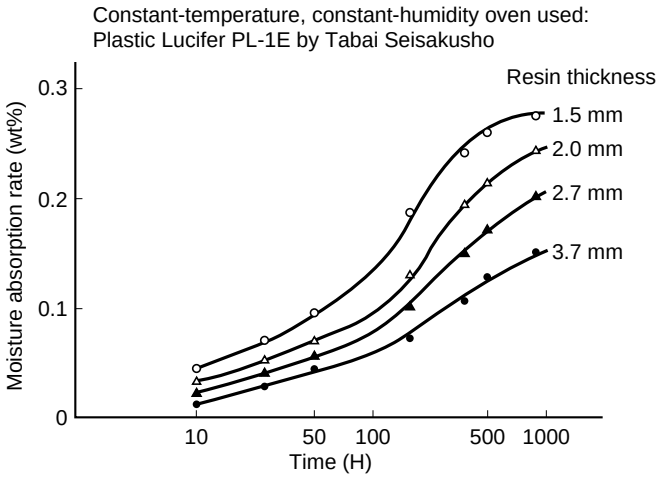
(a) Moisture absorption characteristics at 25°C, 65%

Figure 1-45 shows the moisture absorption characteristics of QFPs of various epoxy resin thickness when the packages are stored at an ambient temperature (T_a) of 25°C and a relative humidity (RH) of 65%.

The vertical axis of this figure indicates the moisture absorbed by the packages divided by the resin weight at the beginning of storage and expressed in percentage. The horizontal axis indicates the lapse of time. As shown in this figure, the moisture absorption rate varies depending on the thickness of the resin, i.e., the thinner the package, the quicker the package absorbs moisture.

It is recommended that NEC's packages be stored at 25°C, 65% RH after the dry pack was opened.

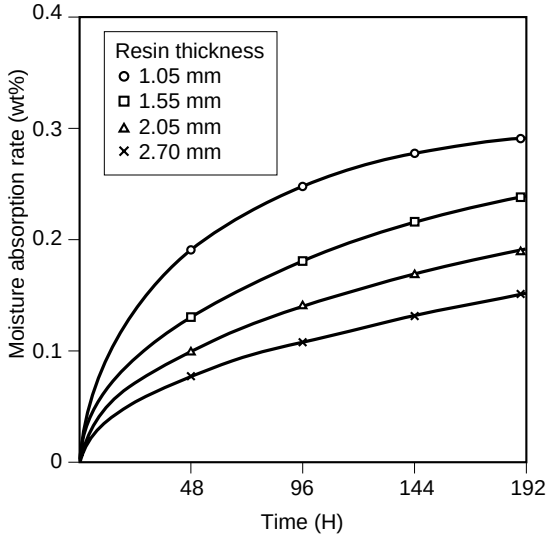
Figure 1-45. Moisture Absorption Characteristics at 25°C, 65% RH



(b) Moisture absorption characteristics at 30 °C, 70% RH

Figure 1-46 shows the result of moisture absorption characteristic simulation (calculated value) at 30°C, 70% RH. NEC conducts its humidification processing test at 30°C, 70% RH on the products for which moisture absorption must be controlled. This condition complies with the EIAJ (Electronic Industries Association of Japan) standard (30°C, 70% RH: moisture absorption control necessary).

Figure 1-46. Moisture Absorption Characteristics at 30°C, 70% RH (calculated value)

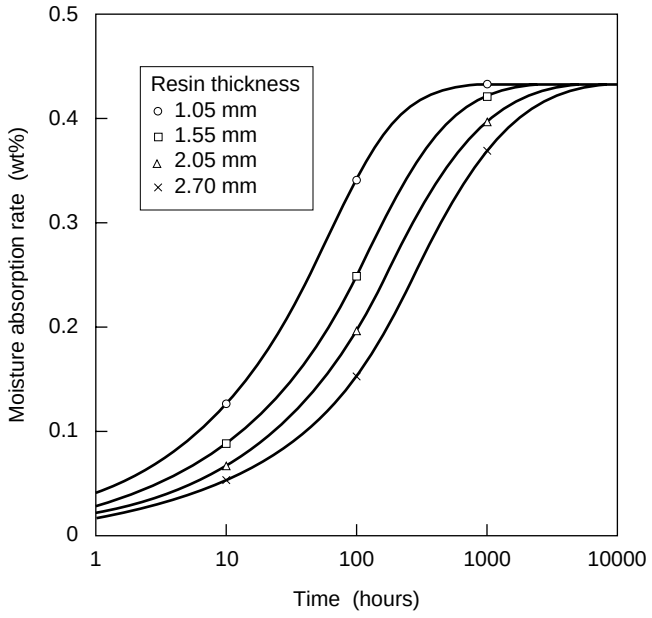


(c) Moisture absorption characteristics at 30°C, 85% RH

Figure 1-47 shows the result of moisture absorption characteristic simulation (calculated value) at 30°C, 85% RH. NEC conducts its humidification processing test at 30°C, 85% RH on the products for which moisture absorption control is not necessary. This condition complies with the EIAJ standard (30°C, 85% RH: moisture absorption control is unnecessary).

Because it takes a long time to test under conditions of 30°C, 85% RH, the test time is shortened by actually conducting an equivalent test at 85°C, 85% RH so that the same amount of moisture is absorbed.

Figure 1-47. Moisture Absorption Characteristics at 30°C, 85% RH (calculated value)



(d) Drying temperature characteristics

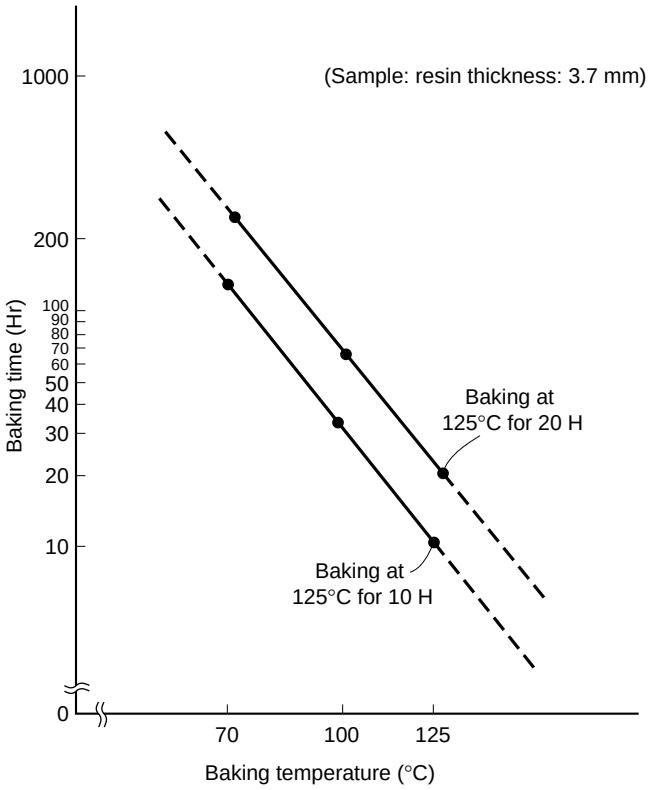
Figure 1-48 shows the moisture absorption of a sample equivalent to when the sample is baked at 125°C for 10, 16, and 20 hours, respectively, when the sample is baked at the lower temperatures.

This data is shown for your reference if you need to bake at the lower temperatures. As shown, the baking time at 90°C is about seven times that at 125°C. If the sample is baked at 70 °C, the baking time is about 15 times longer than at 125°C.

Note that if the sample is baked at 70 °C, and when the moisture absorption rate has dropped below 0.1 wt%, the sample cannot be dried further depending on the environments.

Also note that too long a baking time may cause oxidization of the leads.

Figure 1-48. Drying Characteristics



1.3.2 Reliability of soldering

(1) Exterior plating

A semiconductor device is usually mounted on a PWB by means of soldering or with a socket. At this time, the surface characteristics of the external pins of the device must satisfy these conditions:

<1> Good electrical conductivity

<2> Good solderability, i.e., good mechanical connection

<3> Pin materials highly resistant to corrosion

To satisfy the above three requirements, the external pins of semiconductor devices are solder-plated as surface processing.

Table 1-17 lists types of metal surface processing and their features. As is evident from this table, solder plating is the most excellent surface processing of all, and the most popular plating film provided to the external pins of semiconductor devices. The color tone of this plating film is mainly matt or semi-gloss.

Table 1-17. Metal Surface Processing and Solderability

Surface processing	Solderability	Dirt of solder	Long-time reliability	Cost	Other
Gold plating	◎	△	◎	×	Degraded mechanical durability; Excellent electric conductivity
Silver plating	◎	◎	△	○	Excellent mechanical durability
Tin plating	◎	◎	△	△	Unstable; Aging
Cadmium plating	◎	△	△	△	Mechanically weak film; Easy to collect dirt
Copper plating	○	○	×	○	Easy to oxidize
Nickel plating	×	○	○	○	Active flux necessary
Application of protection film	○	○	△	○	Acid cleaning for copper or brass with flux applied
Solder dip	◎	◎	○	○	Preliminary solder dipping
Electrolytic solder plating	◎	◎	◎	○	

◎ ... Excellent, ○ ... Good, △ ... Fair, × ... Poor

(2) Features of NEC's exterior plating

NEC applies the following solder plating specifications to its semiconductor devices and carries out control so that sufficient solderability is realized:

- Composition ... Sn/Pb = 90/10 to 70/30
  <Reason>

<1> To conform to MIL-M38510E, F specification (The ratio of Pb must be 2 to 50%.)

<2> To prevent generation of whisker which is a needle-like crystal measuring several to several 10s microns growing from plating film (single crystal of Sn) and may short-circuit the pins of the semiconductor device, causing malfunctioning. The whisker is considered likely to occur with Sn plating.

<3> To obtain favorable result of solderability test. One of the parameters of the solderability test is "solder wet time".

According to a representative meniscograph test (**Figure 1-49**), the shorter the wet time (B to E), the better. **Figure 1-50** shows the relations between the solder plating composition and wet time.

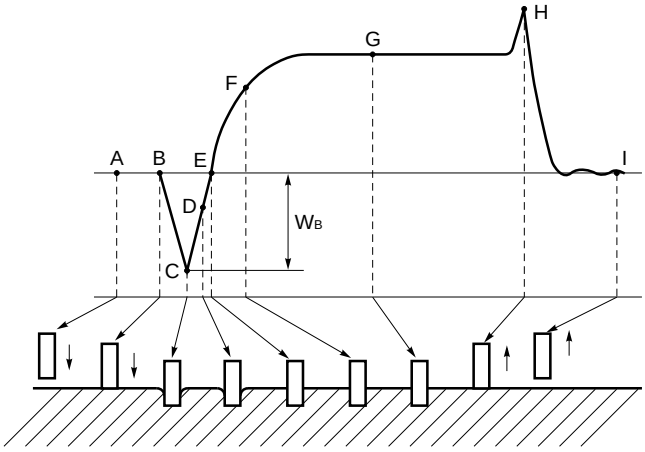
- Plating thickness ... 8 μ typ.
  <Reason>

<1> To conform to MIL-M38510E specification

<2> To stabilize plating film

<3> The plating film is sponge-like, and if the thinner the plating thickness, the more plating pin holes that go through to the substrate, degrading the substrate protection function, solderability, and anti-corrosiveness. **Figure 1-51** shows the relations between semi-gloss solder plating thickness and pin holes.

Figure 1-49. Meniscograph Test



Wet time: B to E
Maximum value of buoyancy: W_B

Figure 1-50. Relations between Plating Composition and Wet Time

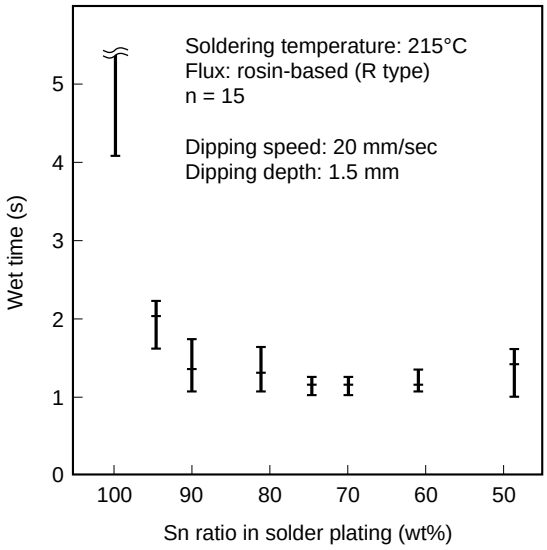
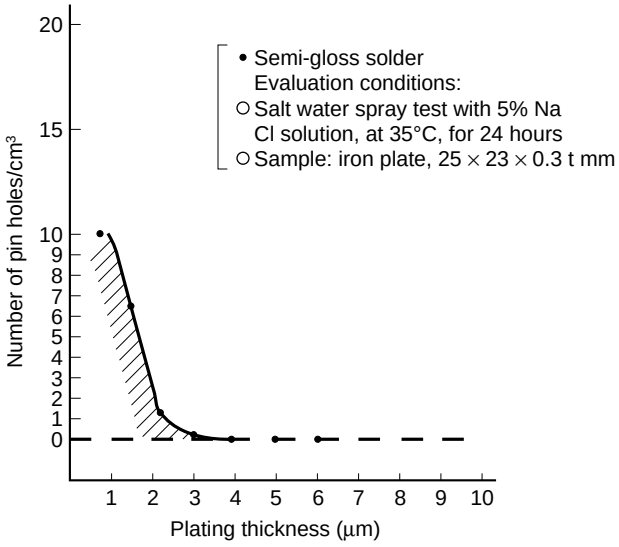


Figure 1-51. Plating Thickness and Pin Hole



As shown in this figure, it is considered that no pin hole is created if the plating thickness is 4 μm or more, and the materials do not rust.

- Color tone ... Matt or semi-gloss

Table 1-18 shows the criteria of solderability. According to this table, a sample with 95% or more of the surface of its leads wetted with solder after the leads have been dipped in solder (230°C) is judged to be acceptable, and a sample with less than 95% of its lead surface wetted is defective.

Table 1-18. Criteria by Wetted Area

Standard	Surface to be soldered	Area wetted with solder	Criteria
A	Smooth and mirror surface	100%	Acceptable
B	Project and recess on surface	100%	Acceptable
C	Small pin holes on surface	95% or more	Acceptable
D	Pin holes through which substrate can be seen exist and part of many edges is not wetted with solder	Less than 95% (70 to 95%)	Defective
E	Pin holes of 0.1 dia. or more exist and most part of edge is not wetted with solder	Less than 95% (70% or less)	Defective

Figure 1-52 shows the result of a solderability test conducted after each solder plating has been aged. Almost no change is observed after the sample has been stored at a temperature and humidity as high as 98°C and 98% RH, respectively, demonstrating stable solderability.

Figure 1-52. Result of Solderability Test of Each Solder Composition after Aging

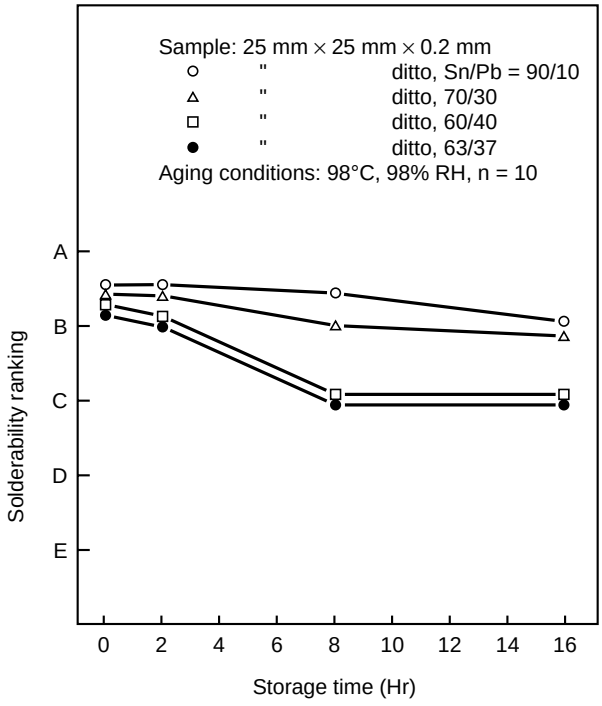


Figure 1-53 shows the result of a test conducted to investigate how solderability differs depending on the pin materials.
The reliability of Cu keeps over a long time, rivaling with the existing 42-alloy (Fe-Ni alloy).

Figure 1-53. Result of Solderability Acceleration Test with Various Pin Materials

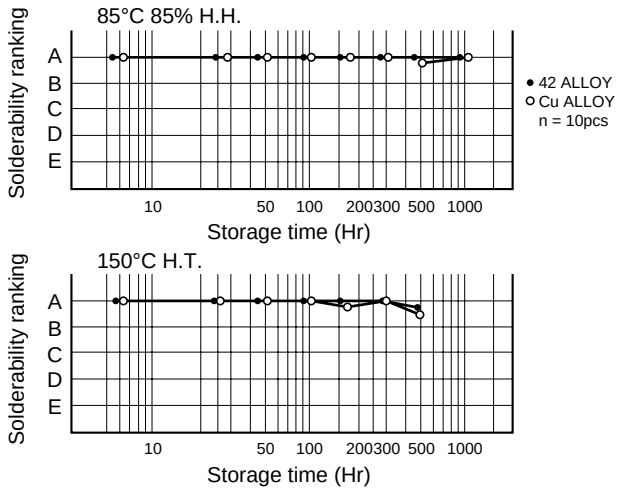


Figure 1-54 shows the relations between baking processing and solderability. This figure indicates that even if re-baking processing is performed after the dry pack has been opened, normal processing (at 125°C for 16 hours) does not cause degradation.

Figure 1-54. Result of Solderability Acceleration Test (125°C HT)

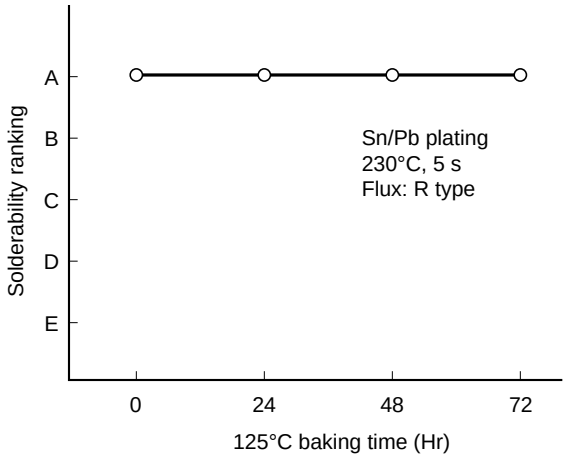
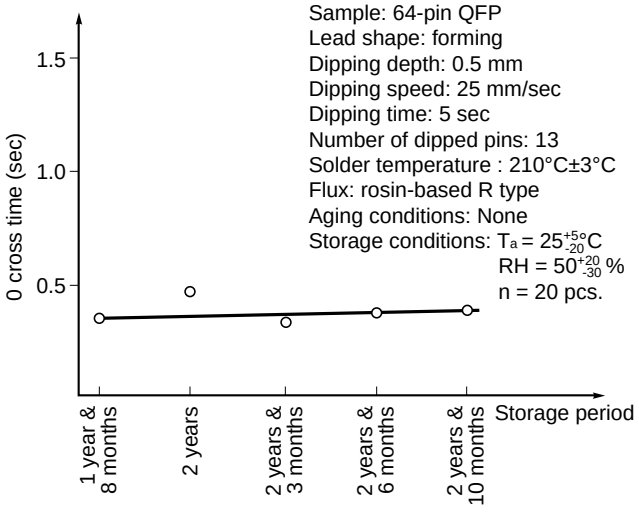


Figure 1-55. Result of Solderability Test on Products Stored for Long Time (Meniscograph method)

[Solderability of product stored for long time]
Figure 1-55 shows the result of evaluation by the Meniscograph method of the products stored in an NEC's warehouse for a long time (up to 3 years). This figure indicates that the good solderability is maintained for a long time.
The above results demonstrate that NEC's IC products have excellent solderability.

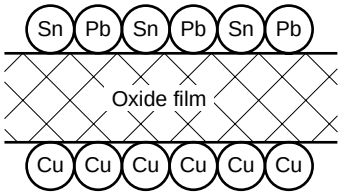


(3) Soldering process

(a) Definition of soldering (courtesy: Senju Kinzoku)

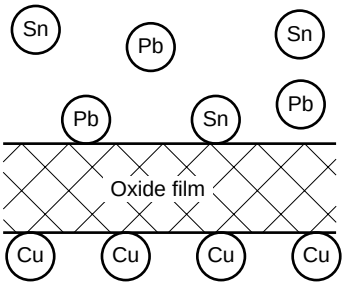
Soldering is a technique to join a metal to another metal by using alloy reaction that takes place between molten solder and the base metal, without the base metal melted.
The following is an example of soldering Cu with Sn-Pb solder:

<1> The surfaces of the solder and base metal are covered with an oxide film.



↓

<2> When the solder is heated and melted, the atoms of Sn and Pb in the solder can move freely. Moreover, the crystal lattice gap of the base metal is also opened as a result of heating, and the atoms of the base metal can easily diffuse into the lattice of other atoms.



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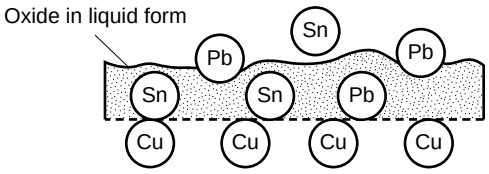
<3> The flux eliminates the oxide film on the surfaces of the solder and base metal, resulting in direct collision between the atom of the solder and atom of the base metal.



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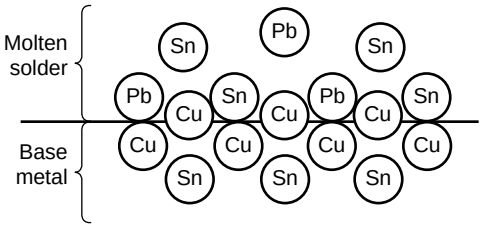
<4> Sn in the solder diffuses into the base metal, creating an alloy layer between the base metal. At the same time, the base metal atom is melted into the molten solder.



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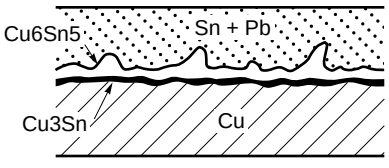
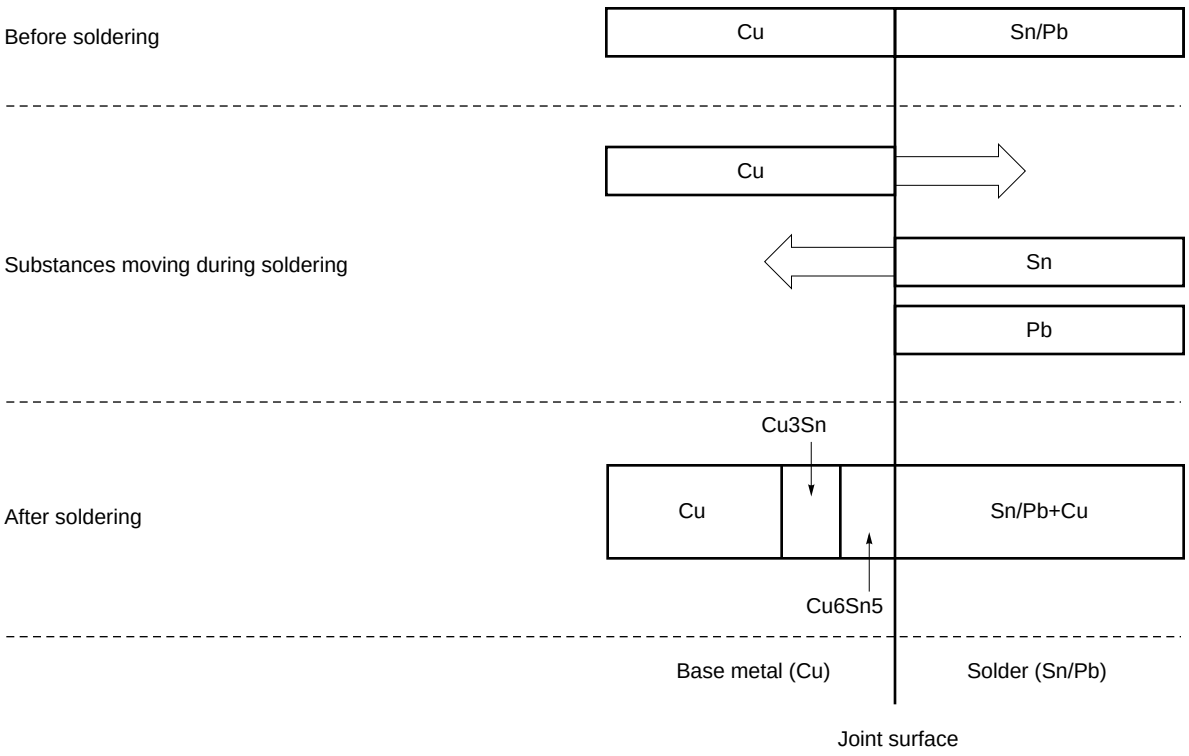
<5> An alloy layer is created. When this layer has been cooled, soldering is completed.



The movements of the metals at the joint surface is as illustrated in **Figure 1-56**.

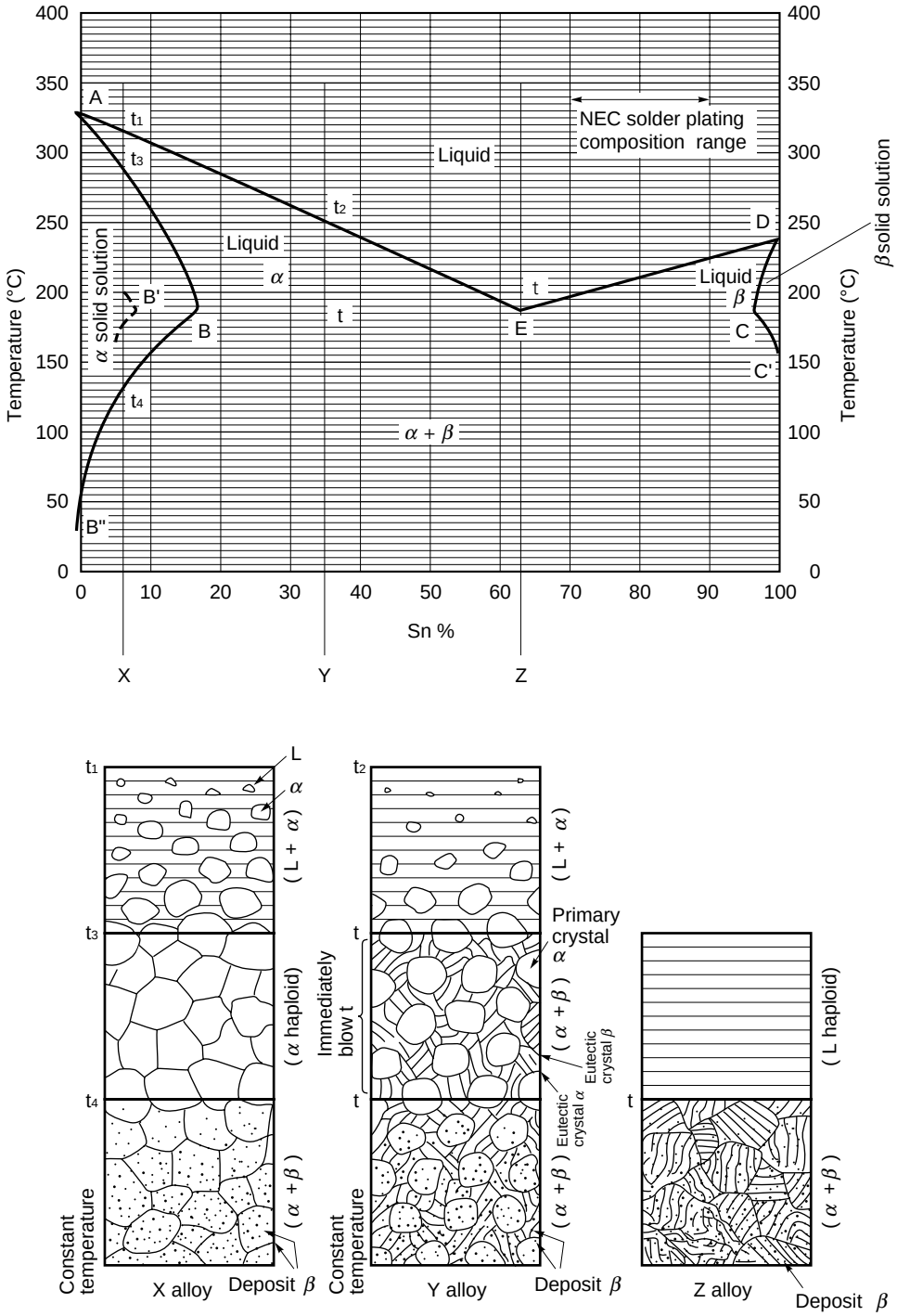
Figure 1-56. Movements of Metal at Joint of Copper Soldering



(b) Sn-Pb alloy status

Figure 1-57 shows how the status of the metal is changed by the alloy ratio of Sn and Pb and temperature, and is called an alloy status diagram.

Figure 1-57. Sn-Pb Alloy Status Diagram



In this diagram,

A to E to D: This curve is called a liquidus line, above which the solder is in the liquid status.

A to B to E, E to C to D: These curves are called solidus lines which indicate temperatures at which the molten solder completely solidifies. The region enclosed by the liquidus line and solidus lines indicates that the solder is in the semi-molten status.

B to E to C: This curve is called a eutectic line. Sn solder (19.5 to 97.5%) starts melting at 183°C.

With NEC's solder plating composition, the liquidus line is in a range of about 192°C to 215°C.

The NEC's solder plating composition provides sufficient wettability even if soldered by means of VPS by which the soldering temperature is the lowest of all the currently available soldering methods (boiling point of 215°C: when Florinate FC70 or Gulden LS215 is used).

The melting point of the solder in actual soldering processing is slightly higher than 183°C.

This is because the quantity of solder in the solder paste (Sn/Pb = 60/40) is much more than the quantity of soldering plate on the pin surface, and during soldering, the solder paste starts melting first, and then the solder plating melts, mixing with the solder paste.

NEC's SMDs, therefore, can be effectively soldered even if the soldering temperature drops below 215 °C.

(4) Factors influencing solderability

Generally, the factors that may influence the solderability when soldering is performed are:

<1> Temperature profile conditions
<2> Warping or waving of PWB
<3> Pin flatness (coplanarity)
<4> Characteristics of solder paste
<5> Quantity of solder paste
<6> Surface conditions of pin
<7> Surface conditions of mounting pad

The pin flatness of NEC's QFP is guaranteed to be 0.15 mm MAX. or that of 0.5 mm pitch QFP is 0.10 mm MAX., and that of 0.4 mm pitch QFP is 0.08 mm MAX.

Therefore, the thickness of the solder paste to solder these QFPs effectively must be 0.20 mm for 0.15 mm MAX., and 0.15 mm for 0.10, 0.08 mm MAX. because of the relations with <1> warping and waving of PWB and <2> pin flatness (coplanarity).

The quantity of the solder paste must be optimized through soldering evaluation by changing the application area (mounting pad dimensions and area of the opening of the screen) and thickness (screen thickness), so that solder bridge or cold solder does not occur.

If impurities are mixed with the solder paste, or if the characteristics of the solder paste degrade, the solderability may be significantly affected. **Table 1-19** shows the permissible quantity and influences of impurities.

Table 1-19. Permissible Quantity and Influence of Impurities

Courtesy: Senju Kinzoku

Element	Permissible value (wt%)	Source	Influences
Zn	0.005	Soldered material (brass)	Solder surface is easy to oxide, causing icicle and bridge. Soldered surface turns white.
Cu	0.3	Soldered material	Cu_6Sn_5 metal compound generated, causing icicle and bridge. Strength increases.
Ag	—	ditto	Solidus line lowered by 3 to 5°C. Soldered surface turns white at around 0.1%. Fair wettability. Strength increases.
Au	—	ditto	Strength drops during soldering to Au plating. Soldered surface turns white.
Fe	—	ditto, solder bath material	Difficult to melt with solder. Metal compound generated.
Ni	—	ditto	ditto
Sb	1.0	Solder	Wettability degraded. Electric resistance increases. Strength increases. Glittering surface.
Bi	0.3	ditto (low-temperature soldering)	Solidus line lowered. Solder becomes hard and easy to break. Matt soldered surface.
Cd	0.2	ditto (ditto)	Solidus line lowered. Wettability degraded.

1.4 Recommended Conditions

This section introduces the soldering conditions and cleaning conditions recommended by NEC.

1.4.1 Recommended soldering conditions

(1) NEC's concept of recommended conditions

NEC specifies the recommended soldering conditions for each of its products.

This is because the quality of each SMD is heavily influenced by different degree of the following factors, as described in the preceding section:

<1> Moisture absorption of package (storage conditions)

<2> Soldering conditions (method and conditions)

<3> Package structure (thickness, chip size, etc.)

Therefore, NEC specifies the recommended soldering conditions of each product, without classifying its products by groups of products (such as memories or microcomputer) and packages (such as SOP and QFP).

(2) Classification of recommended soldering conditions

NEC's recommended soldering conditions can be broadly classified into <1> heating conditions of soldering method, <2> package moisture absorption control, and <3> number of times the product is to be mounted. NEC's basic classification of soldering methods and the recommended soldering conditions are shown in **Table 1-20**.

Figure 1-58. Recommended Temperature Profile of Infrared Reflow (Peak Temperature: 230˚C)

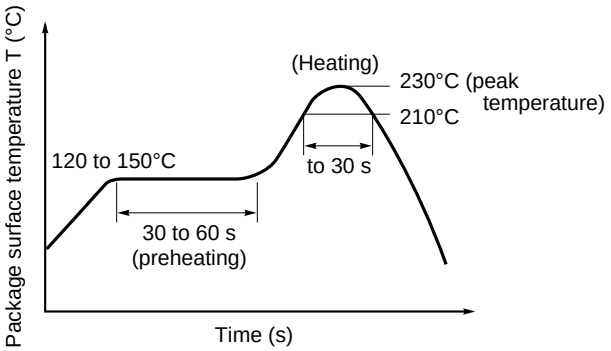


Figure 1-59. Recommended Temperature Profile of Infrared Reflow (Peak temperature: 235˚C)

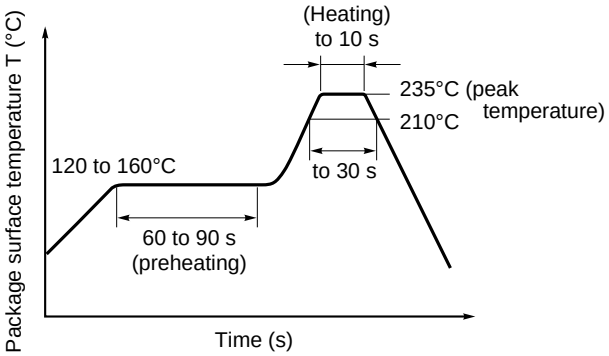


Figure 1-60. Recommended Temperature Profile of Infrared Reflow (Peak Temperature: 220˚C)

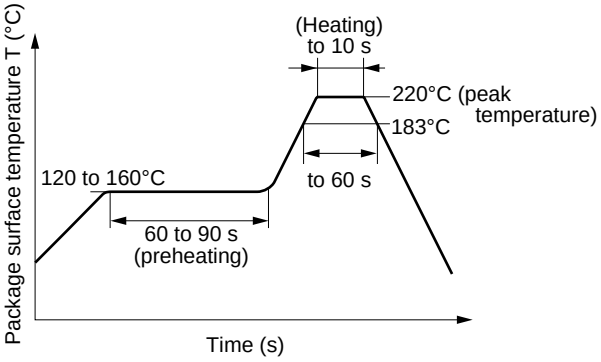


Figure 1-61. Recommended Temperature Profile of VPS Reflow

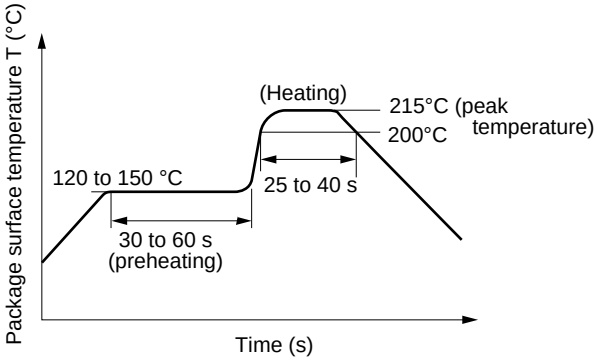


Table 1-20. Classification of Soldering Methods and Recommended Soldering Conditions

Division	Soldering method	Recommended soldering conditions	Recommended temperature profile	Remarks
Whole heating method	Wave soldering	• Peak temperature: 260°C (molten solder temperature) • Soldering time: 10 s MAX. • Preheating conditions: 120°C MAX. (package surface temperature), no time limit • Number of times: 1	———	Temporarily fixed on PWB
	Infrared reflow soldering (IR) Note 1	• Peak temperature: 230°C (package surface temperature) • Time of temperature higher than 210°C: 30 s MAX. • Preheating conditions: 120 to 150°C (package surface temperature), 30 to 60 s • Number of reflows: 1, 2 or 3 Note 2	**Figure 1-58**	Including hot air reflow soldering
		• Peak temperature: 235°C (package surface temperature) • Time of temperature higher than 210°C: 30 s MAX. • Preheating conditions: 120 to 160°C (package surface temperature), 60 to 90 s • Number of reflows: 1 or 2 Note 2	**Figure 1-59**	
		• Peak temperature: 220°C (package surface temperature) • Time of temperature higher than 183°C: 60 s MAX. • Preheating conditions: 120 to 160°C (package surface temperature), 60 to 90 s • Number of reflows: 1, 2 or 3 Note 2	**Figure 1-60**	———
	Vapor phase reflow soldering (VPS)	• Peak temperature: 215°C (package surface temperature) • Time of temperature higher than 200°C: 40 s MAX. • Preheating conditions: 120 to 150°C (package surface temperature), 30 to 60 s • Number of reflows: 1, 2 or 3 Note 2	**Figure 1-61**	———
Partial heating method	By laser or soldering iron Note 3	• Peak temperature: 300°C (pin temperature) • Time: 3 s MAX. (per side of device)	———	———

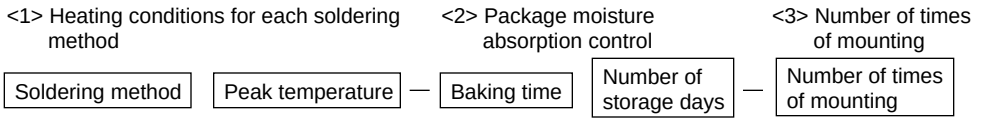
Notes 1. The recommended peak temperature for infrared reflow soldering is either 220°C, 230°C or 235°C depending on the products. For details, consult NEC.

2. The number of times the product can be mounted is either once, twice or three times depending on the products. For details, consult NEC.

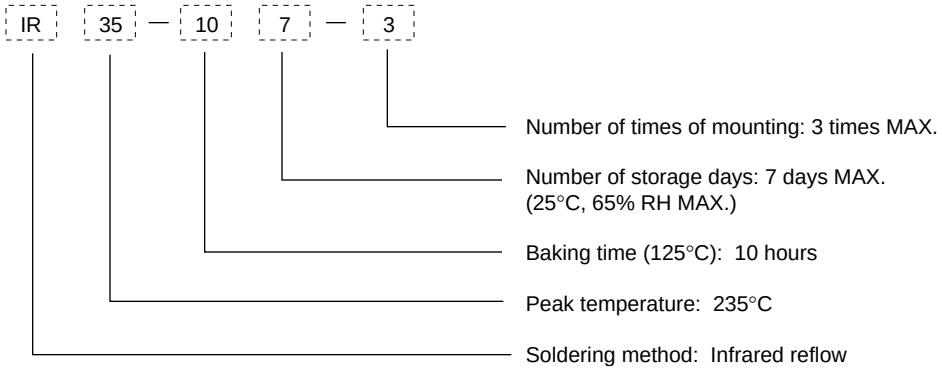
3. For details on the partial heating method, refer to section **1.2.6 Soldering method**.

(3) Symbol code of recommended soldering conditions

The symbol code indicating NEC's recommended soldering conditions include codes indicating <1> heating conditions of each soldering method and <2> package moisture absorption control.
In addition, these codes also include those indicating the soldering method, peak temperature, baking time, the number of storage days after the dry pack has been opened, and the number of times the product can be mounted. These symbol codes are used in combination as follows:



(Example)



[Soldering method]

The soldering method is indicated by a code consisting of two alphabetic characters, as shown in the table on the right.

Symbol	Soldering method
IR	Infrared reflow
VP	VPS
WS	Wave soldering

[Peak temperature]

The peak temperature is indicated by the lower two digits of the specified peak temperature (e.g., if the specified peak temperature is 235°C, code "35" is indicated). Note that the package surface temperature is indicated if the recommended soldering method is infrared reflow or VPS, and that the molten solder temperature is indicated if the soldering method is wave soldering.

Symbol	Peak temperature
15	215°C
20	220°C
30	230°C
35	235°C
60	260°C

[Baking time]

The recommended baking time is indicated by using the symbols, each consisting of two digits of numeral, shown in the table on the right.

Symbol	Baking time (when stored at 125°C)
00	Baking unnecessary (0 hour)
10	10 hours MIN., 72 hours MAX.
16	16 hours MIN., 72 hours MAX.
20	20 hours MIN., 72 hours MAX.
36	36 hours MIN., 72 hours MAX.

[Number of storage days after opening of dry pack]

The number of days during which the product can be stored after the dry pack has been opened is indicated by the symbols shown on the right.

Symbol	Number of days (25°C, 65% RH MAX.)
1	1 day (24 hours) MAX.
2	2 days (48 hours) MAX.
3	3 days (72 hours) MAX.
7	7 days (168 hours) MAX.
None	Not limited

[Number of times of mounting]

The number of times the product can be mounted is indicated by the symbols shown on the right.

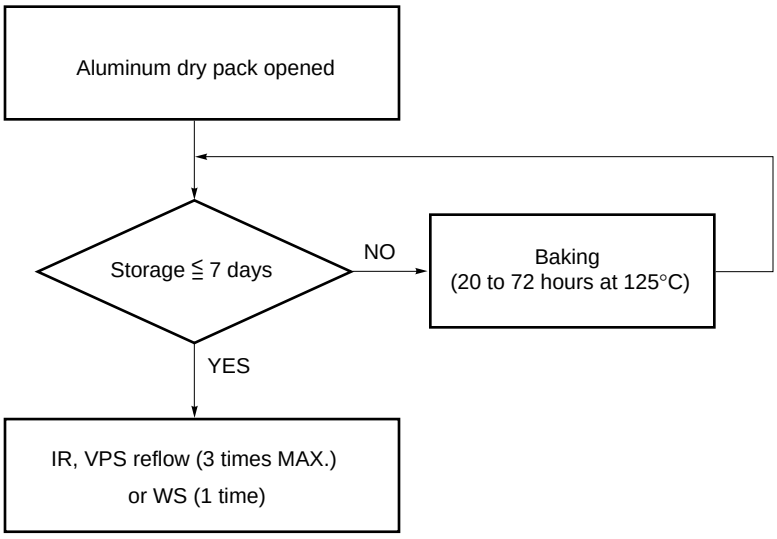
Symbol	Number of times
1	1
2	2 times MAX.
3	3 times MAX.

The above symbol codes apply to the products that can be soldered by means of general heating methods. Some of NEC's SMDs, however, cannot be soldered by general heating method, and a code indicating that these products must be soldered by partial heating method is indicated for such products.
Here is an example of the symbol codes described above:

Part number	Package	Resin thickness	Recommended soldering conditions
μPD78P332GF	80-pin QFP	2.7 mm	IR35-207-3, VP15-207-3, WS60-207-1

The codes in the column of recommended soldering conditions in the above table indicate that the product μPD78P332GF can be stored for 7 days or less after the dry pack has been opened (under storage conditions of 25°C and 65% RH MAX.), can be mounted up to 3 times by infrared reflow (IR) [peak resin surface temperature: 235°C] or vapor phase soldering (VPS) [peak resin surface temperature: 215°C], or once by wave soldering (WS). If the specified storage period has expired, this product must be baked for 20 hours or longer (at 125°C).
The following flowchart, **Figure 1-62**, illustrates this.

Figure 1-62. Flowchart of IR35-207-3, VP15-207-3, WS60-207-1



1.4.2 Recommended conditions of flux cleaning and non-cleaning flux

The conditions of flux cleaning and non-cleaning flux recommended by NEC are as follows:

(1) Recommended flux cleaning conditions

(a) Cleaning solvent

Ethyl alcohol, Methyl alcohol, Isopropyl alcohol,
P3 cold cleaner, Pinealpha ST-100S, Bioact EC-7/EC-7R, Clean through-700 series
Pure water, City water

(b) Cleaning method

<1> Immersion cleaning, rinsing
Solvent temperature: 40°C
Time: 10 minutes MAX.

<2> Ultrasonic cleaning
Solvent temperature: 40°C
Time: 5 minutes MAX.
Frequency: 28 kHz MIN.
Output: 15 W/liter MAX.

(2) Recommended non-cleaning flux

Super low residual flux (ULF-500VS, ULF-210R)
Low residual flux (CF-220V)
Deactive flux (AM-173)
Flux with chlorine content of 0.2 Wt% MAX.

(3) Notes

- Cleaning with fleon-based (including HCFC) and chlorine-based cleaning solvent is not recommended from the viewpoint of environment protection. However, fleon-based solvent, trichloroethylene, and trichloroethane do not affect semiconductor devices if they are used under the above conditions.

- Semiconductor devices are not affected as long as they are cleaned with a solvent at a temperature of 70°C or lower. Some solvents, however, do affect the devices if their temperature rises.

- After cleaning a device, do not touch the device until it dries up because the marking on the device may be erased.

- When using ultrasonic cleaning, be careful about the following.
  Semiconductor devices may be damaged if they directly contact with a resonator.
  If hollow package products (such as ceramic package and canned case) are cleaned by means of ultrasonic cleaning, the bonding wire may break.

- Solder waste or impurities may cause degradation of insulation or characteristics. Perform evaluation by using an appropriate PWB to confirm that no problem occurs.

1.5 Example of Mounting Evaluation of SMDs

1.5.1 Evaluation example of gullwing lead soldered joint

SMDs are usually soldered by means of reflow soldering. Depending on the temperature profile conditions, however, the reliability of the SMDs may be degraded as described in **1.3.1 Resistance to soldering heat**.

On the other hand, however, lowering the reflow temperature profile may degrade the solderability.

This section introduces an example in which NEC's QFPs (with gullwing leads) were soldered at a temperature lower than that recommended by NEC, and then the soldering strength was evaluated, and an evaluation example of the soldered joint using a PWB.

(1) Example of evaluation of soldering strength

Figure 1-63 shows the result of a tensile test in which the pin of the sample was pulled upward in the vertical direction, until they came off. **Figure 1-64** outlines the method of this tensile test.

Figure 1-63. Relations between Reflow Temperature and Soldering Strength

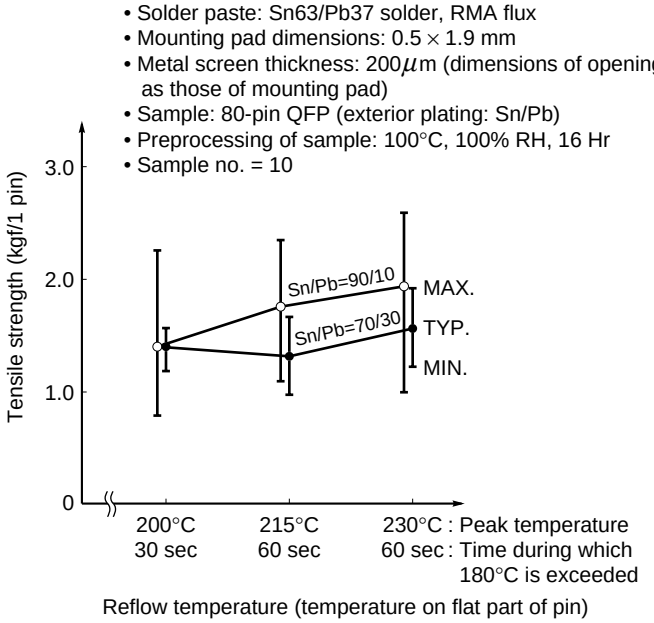
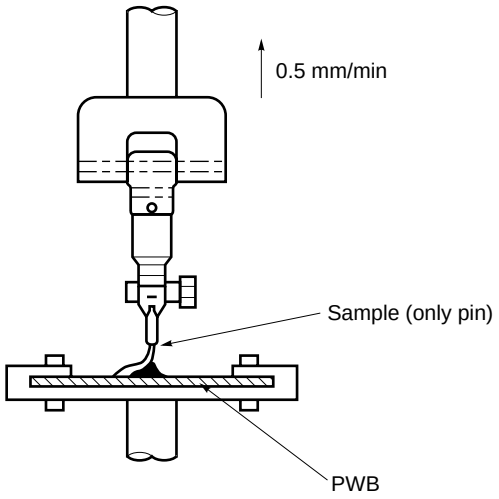


Figure 1-64. Outline of Tensile Test



As shown in **Figures 1-65** and **1-66**, there are some relations between the shape of cross section of the soldered joint and "displacement curve". That is,

<1> The peak strength is obtained when portion A, i.e., the solder fillet created on the bending portion of the pin (heel fillet) is destroyed.

<2> The strength of the flat part of the pin is related to portion B, i.e., the bottom surface of the pin, and is a low value.

<3> The strength of the fillet created at portion C is extremely low, but slightly appears on the displacement curve.

From these results, it is considered that the tensile strength is governed by the shape of the solder fillet (heel fillet), which should be analyzed further.

From the viewpoint of the peak value of tensile strength, however, every part of the pin has a strength of 1 kgf/1 pin MIN., which is considered to be a stable soldering strength.

It can be therefore concluded that even if the temperature profile conditions for reflow soldering are lowered, NEC's SMDs can provide stable soldering strength, as shown in **Figure 1-63**.

Figure 1-65. Relations between Strength of Soldered Joint and Displacement Curve in Tensile Test of QFP (with gullwing lead)

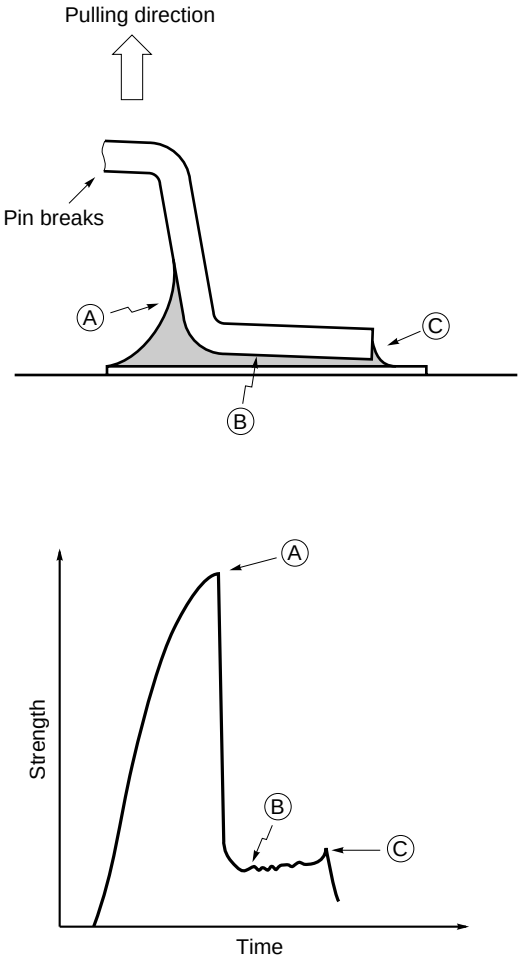


Photo 1-2. Example of Soldering QFP (with gullwing lead)

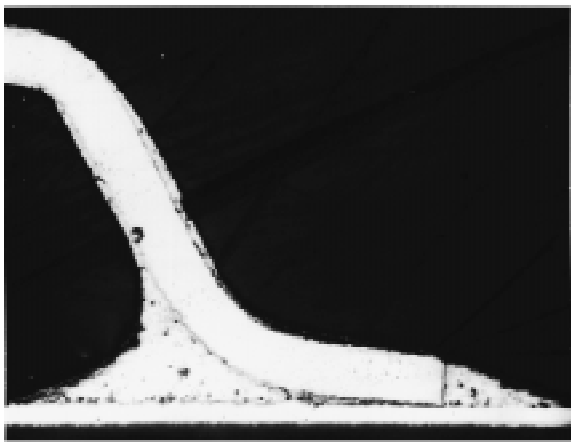
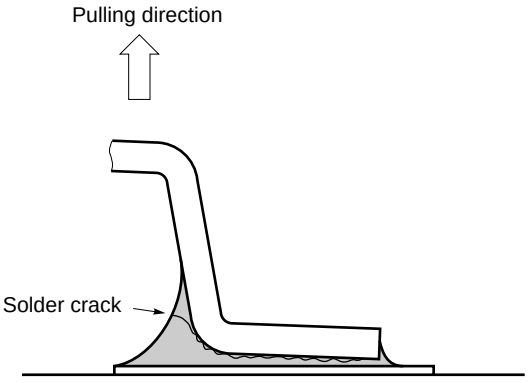


Figure 1-66. Solder Crack Occurrence Position as Result of Tensile Test



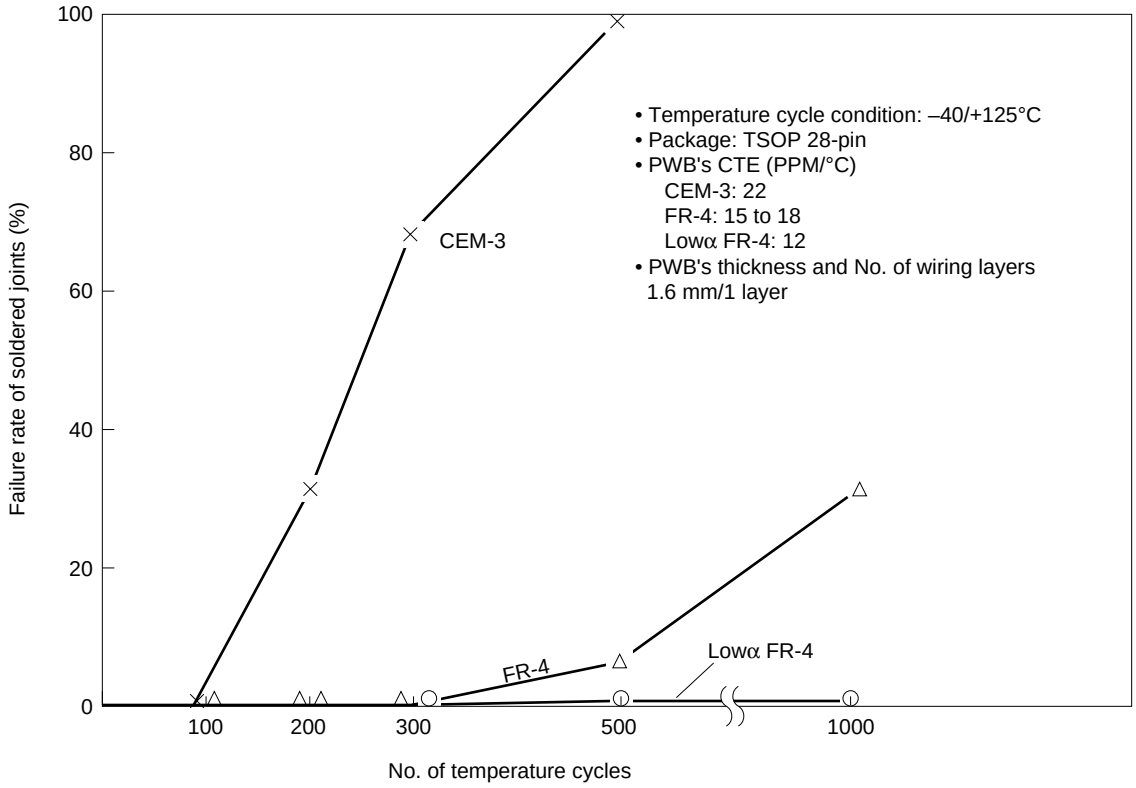
(2) Example of evaluation of soldered joints for printed boards

This section introduces an example in which a 28-pin TSOP is soldered to three PWBs each having a different coefficient of thermal expansion (CTE). **Figure 1-67** shows an example of evaluation of the reliability of soldered joints using temperature cycle testing.

Figure 1-67 shows that soldered joint reliability is greatly influenced by a PWB's CTE, and that it is greatly improved when the PWB's CTE is reduced to 12 PPM.

Therefore, in selecting PWBs, it is necessary to take into consideration whether the parts to be mounted and the PWB's CTE are compatible.

Figure 1-67. Reliability of Soldered Joint Using PWB



1.5.2 Example of improved toe fillet of lead by N_2 reflowing

N_2 reflowing which improves solderability by filling the infrared reflow with nitrogen (N_2) is becoming increasingly widespread. The following describes an example of an improved toe fillet of lead by N_2 reflowing.

Figure 1-68 compares the distribution of the toe fillet height when QFP is mounted with the reflow containing air and with the reflow containing nitrogen (N_2).

The results show that when the reflow contains air, the height of the toe fillet which is less than 1/2 of the thickness of the pin is 60% of the whole area. When the reflow is filled with nitrogen (N_2), the fillet is formed for the whole thickness of the lead. **Photo 1-3** shows the cross-section after mounting when the reflow contains air and when it contains nitrogen (N_2).

Figure 1-69 shows the tensile strength when the toe fillet of lead is present and absent. It shows that the presence of the toe fillet of lead does not affect the tensile strength peak value. From the above results, it indicates that N_2 reflowing is effective for improving the toe fillet of lead.

Figure 1-68. Distribution of Soldering Fillet Height

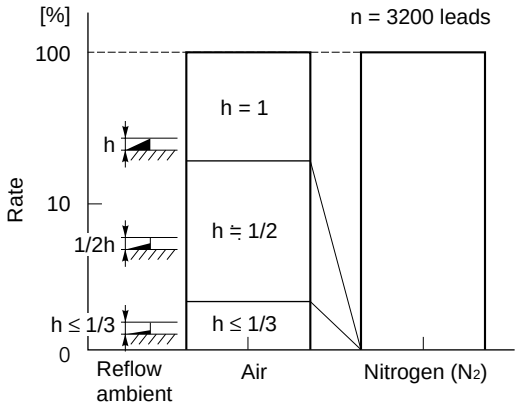


Figure 1-69. Relation Between Toe Fillet and Strength

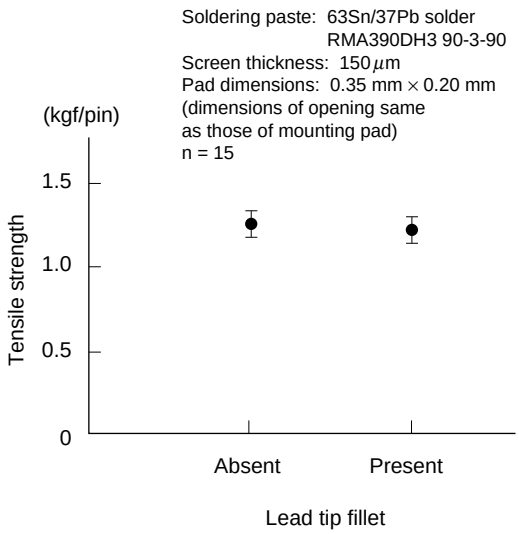
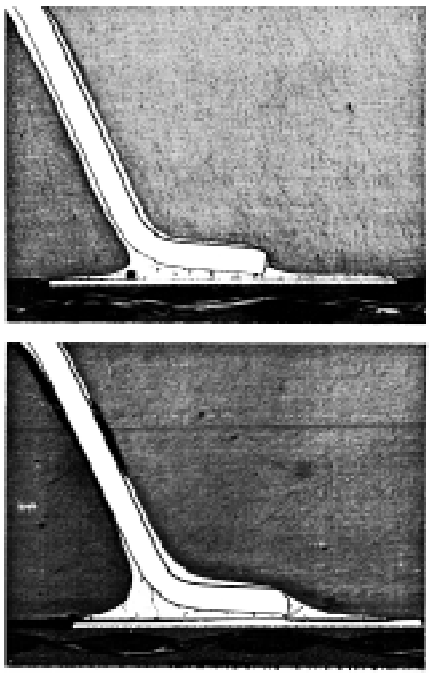


Photo 1-3. Cross-Section After Mounting



Reflow ambient : Air

: Nitrogen (N_2)

Mounting sample: 0.65 mm pitch QFP
Mounting pad dimensions: 0.35 (W) × 2.1 (L) mm
Screen thickness: 150 μm

1.5.3 Evaluation example of mounting fine-pitch QFPs

This section introduces the results of experiments conducted to evaluate the “solder paste printing technology” and “soldering technology” currently used to mount the fine-pitch QFPs.

In applying this technology to the actual production line, it is recommended that these mounting technology factors be taken into consideration and that evaluation be made in accordance with the facility and equipment to be used.

(1) Evaluation example of mounting 0.5-mm pitch QFP

(a) Printability of solder paste

To select solder pastes with excellent solder paste printability, an evaluation was conducted,by using a 150 *m*m metal screen, as illustrated in **Figure 1-70** Outline of Printing Solder Paste, by varying parameters such as <1> clearance between the screen and PWB, <2> impression, and <3> squeegee moving speed. As a result, “Sn63/Pb37 RAM390DH3 90-3-90” by Alphametals, “63-101F-70-9” by Senju Kinzoku, and “CCR63-M102” by Matsuo Handa were considered to be favorable.

Note Recently, however, the above solder pastes have been further improved and excellent solder pastes have been developed by manufacturers not listed in **Table 1-21**. For details, consult each solder paste manufacturer.

Figure 1-70. Outline of Printing Solder Paste

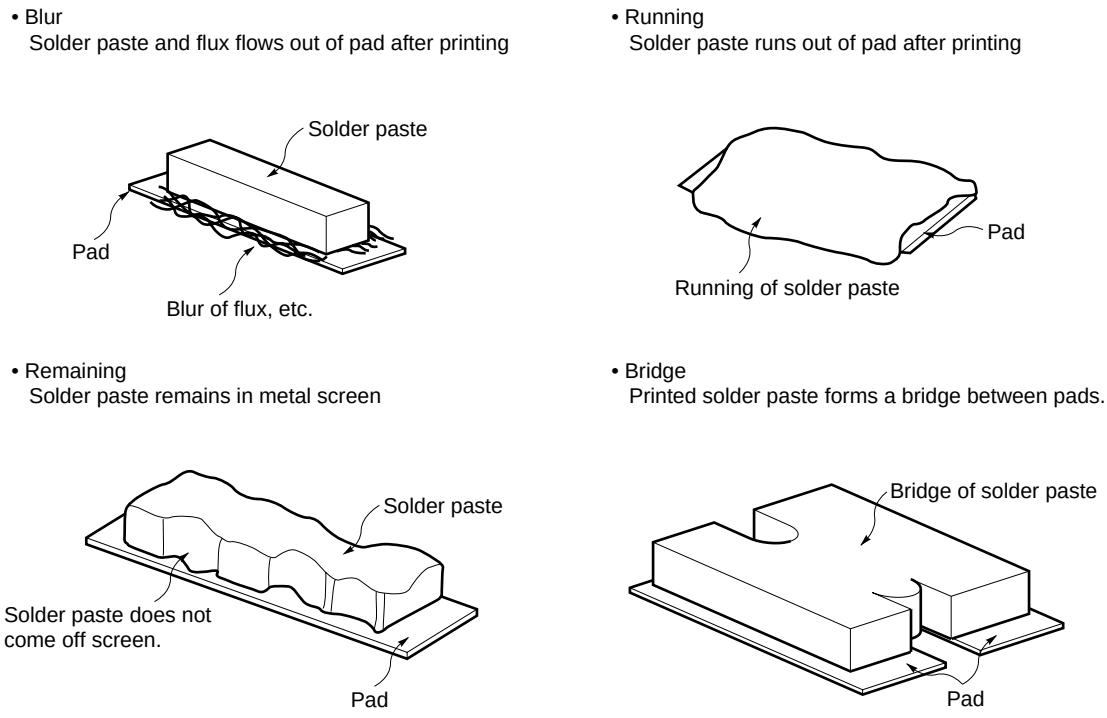


Table 1-21. Result of Evaluation of Solder Paste Printability

Manufacturer	Part number	Blur	Remaining	Running	Bridge	Solder powder content (%)	Viscosity (CPS)	Solder powder grading (mesh)	cl content (%)	Solder powder grading shape
Alphametals	63/37 RMA390 DH3	△	○	○	○	90	90×10^4	325 ~	0	Ball-shaped
Senju Kinzoku Kogyo	63-101F-70-9	△	○	△	△	?	40 to 50 $\times 10^4$ HBT	200 ~	0.2	Ball-shaped
Matsuo Handa	CCR63-M102	△	○	○	○	87.8	105×10^4 (BH)	400 to 500	0.2	Ball-shaped

○: Good, △: Fair, ×: Poor, —: Cannot be printed, Screen: evaluated by SUS

There is a report that phosphor bronze and a metal created by additive method are better than stainless steel as the materials of a metal screen for solder paste printing. When using a screen for fine-pitch pattern, consult screen manufacturers.

(b) Evaluation example of soldering 0.5-mm pitch TQFP

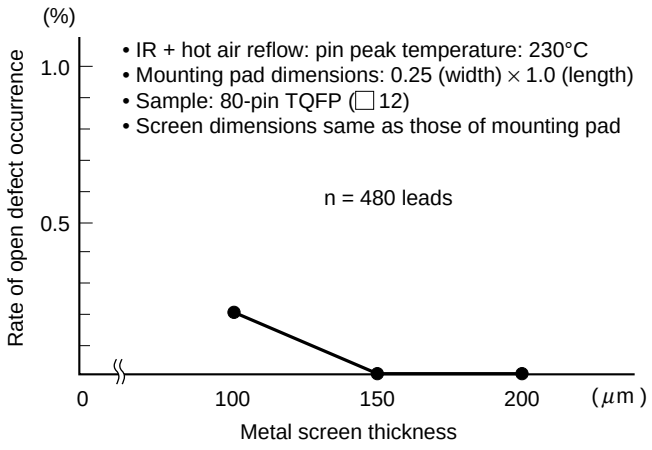
The sample to be evaluated was an 80-pin TQFP (□12) plastic package. In this experiment, the screen thickness, mounting pad dimensions and the reflow temperature were varied to evaluate the soldering technology.

<1> Screen thickness

Figure 1-71 shows the result of a test conducted to investigate the rate of occurrence of open defect when the sample was soldered with various metal screens with different thickness.

This figure indicates that stable solderability can be obtained when the sample, having a pin pitch of 0.5 mm, is soldered with a metal screen 150 to 200 μm thick.

Figure 1-71. Rate of Open Defect Occurrence of TQFP (0.5-mm pitch)



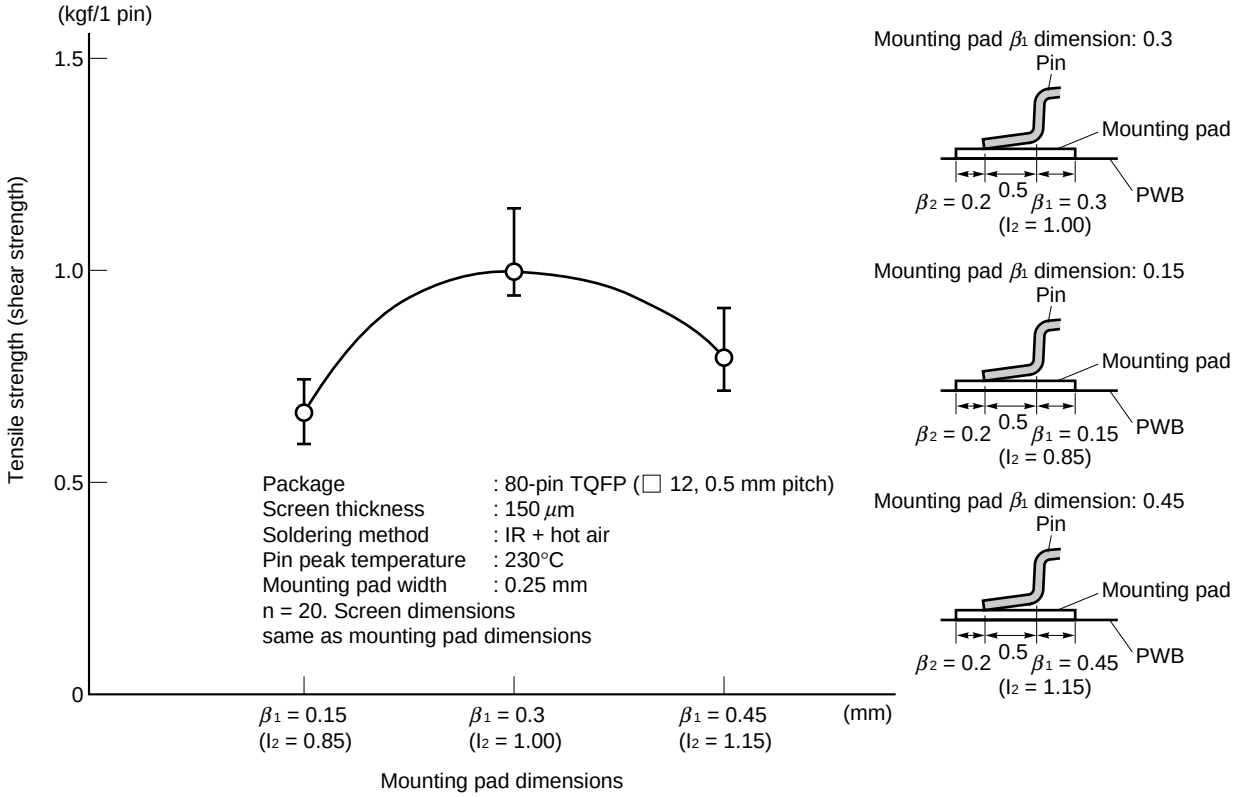
<2> Mounting pad dimensions

Figure 1-72 shows the relations between the mounting pad dimensions (l_2) and the tensile strength of the pins after the sample has been mounted by means of reflow soldering.

This figure indicates that the tensile strength changes with dimension β_1, and that the mount a pad dimension (l_2) of 1.00 mm is appropriate.

(For the relations between β_1 and l_2, refer to the relations between mounting pad dimensions and strength in the same figure.)

Figure 1-72. Relations between Mounting Pad Dimensions and Tensile Strength



<3> Reflow temperature

Figure 1-73 shows the relations between the reflow temperature (pin temperature) and tensile strength.

This figure indicates that stable strength can be obtained if the pin is soldered at 200°C or higher.

Figure 1-73. Relations between Soldering Temperature and Strength

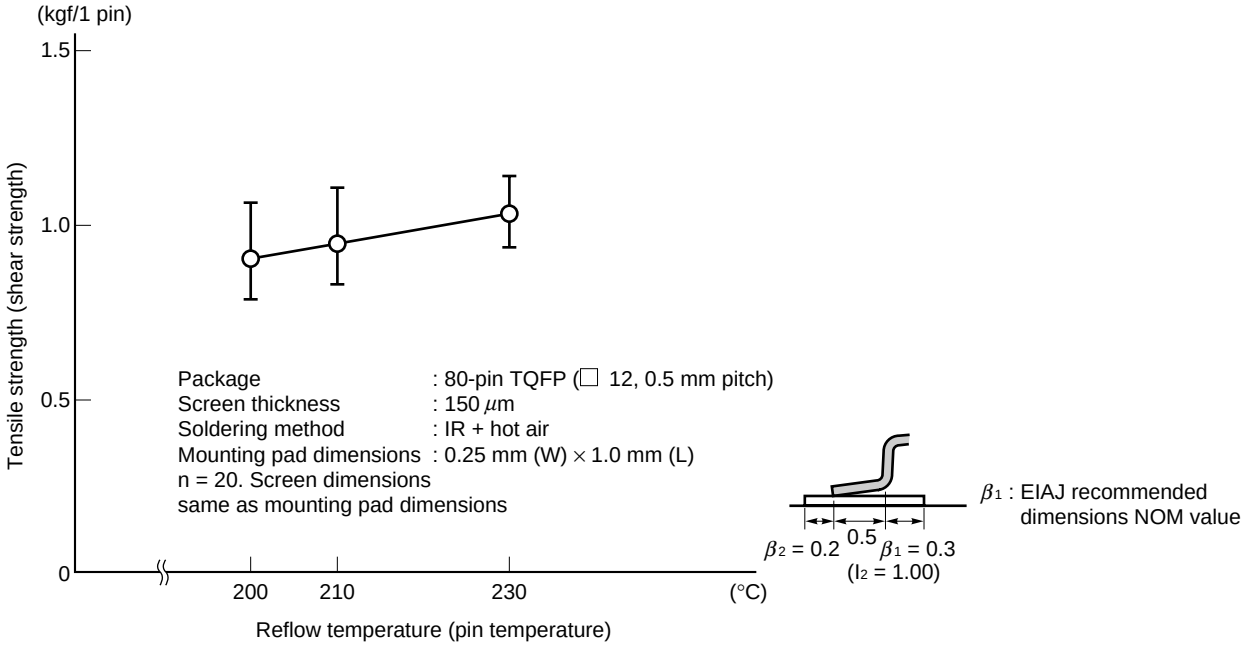


Table 1-22 shows the results of the above experiments <1> through <3> and excerpts of **Table 1-21**, "Result of Evaluation of Solder Paste Printability."

Table 1-22. Results of Evaluating 0.5-mm Pitch TQFP

Parameter	Result
Mounting pad dimensions	β_1 should be 0.3 mm. Pad dimensions for this experiment: 0.25 mm × 1.0 mm
Screen thickness	150 to 200 μm. Dimensions of metal mask opening same as those of mount pad
Solder paste	No difference observed among following three types: <1> Alphametals “63/37 RMA 390DH3 90-3-90” <2> Senju Kinzoku “63-101F-70-9” <3> Matsuo Handa “CCR 63-102”
Reflow conditions (lead temperature)	IR 200 to 230°C

(2) 0.4-mm pitch QFP

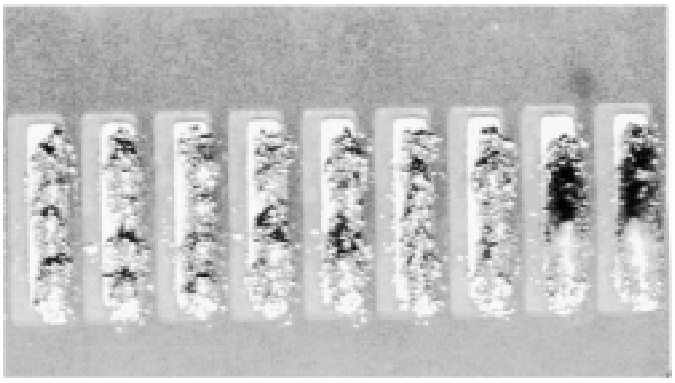
The sample was a 100-pin TQFP (12 x 12 mm) plastic package.
In this experiment, the metal screen thickness was changed to evaluate the printability and solderability. The results of this experiment are compared with those of the experiment with the above mentioned 0.5-mm pitch sample.

<1> Evaluation of printability

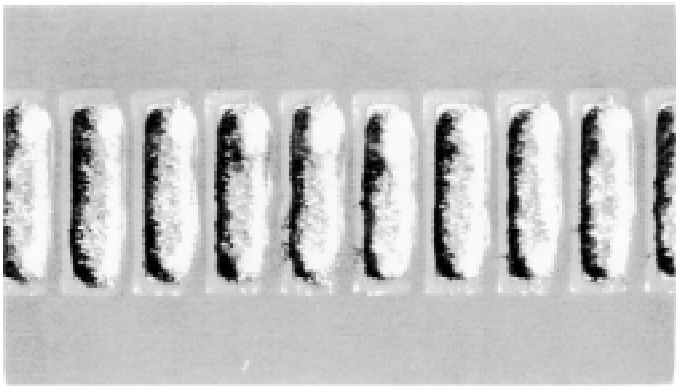
Photo 1-4 shows the appearances of mounting pads printed with metal screens of different thickness. With a screen thickness of 200 μm, the solder paste may remain on the metal screen or blurred on the PWB, and could not be accurately printed. With a screen thickness of 150 μm, however, stable printability was obtained.

Photo 1-4. Appearance of Mounting Pads for 0.4-mm Pitch TQFP

Screen thickness: 200 μm Solder paste: Alphametals “RMA390DH3 90-3-90”



Screen thickness: 150 μm



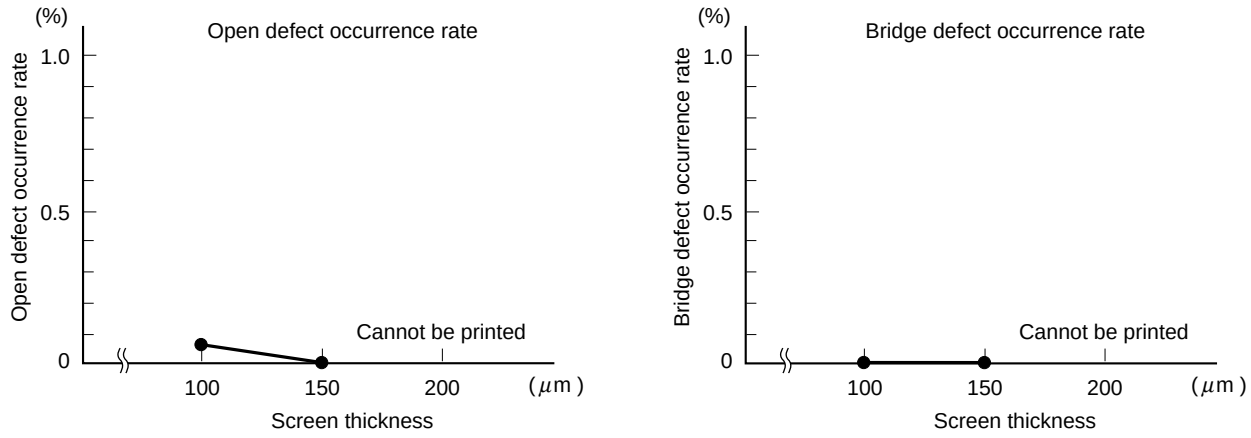
- Mounting pad dimensions: 0.20 (W) $\times$ 1.00 (L) mm
- Screen dimensions are the same as the mounting pad.

<2> Evaluation of solderability

Figure 1-74 shows the rate of occurrence of open and bridges when the sample was mounted with metal screens of different thickness.

This figure indicates that stable solderability is obtained with a screen thickness of 150 μm.

Figure 1-74. Rate of Open and Bridge Defect Occurrence with TQFP (0.4-mm pitch)



Evaluation conditions
Hot air + infrared reflow : pin peak temperature 210˚C
Mounting pad dimensions : 0.20 (W) × 1.00 (L)
Sample : 100-pin TQFP (□12)
Screen dimensions same as mounting pad dimensions
n = 600 leads

From the results of the above experiments <1> and <2>, and by comparing these with the results of the experiments with 0.5-mm pitch sample described above, the following conclusion can be drawn: With the 0.5-mm pitch sample, stable solderability is obtained with a screen thickness of 150 to 200 μm. In contrast, the screen thickness must be 150 μm to solder the 0.4-mm pitch sample.

Photo 1-5 shows a 0.4-mm pitch TQFP solder dimensions and the cross-section.

Photo 1-5. 0.4 mm Pitch TQFP

Photo of solder dimensions

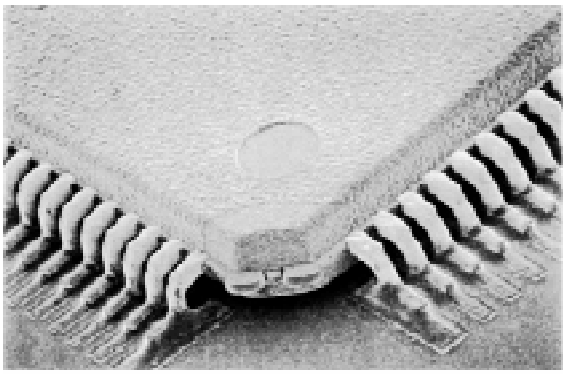
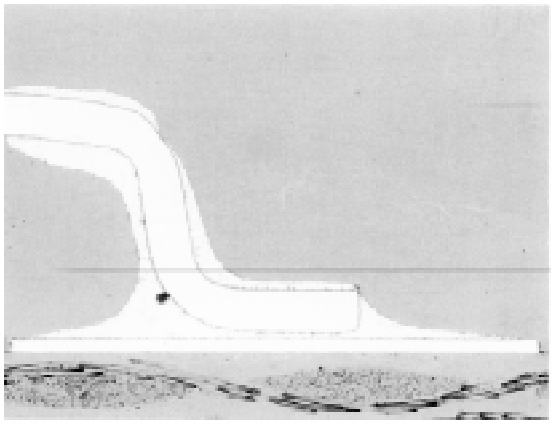


Photo of cross-section



Sample	:	100-pin TQFP
Solder paste	:	63Sn/37Pb RMA390DH3 90-3-90
Mounting pad dimensions	:	0.20 (W) × 1.0 mm (L)
Lead peak temperature	:	230˚C
Metal screen thickness	:	150 μm

Screen dimensions same as mounting pad dimensions

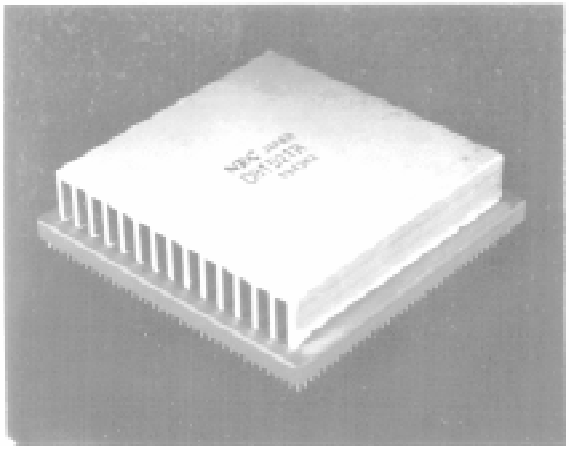
1.5.4 Evaluation example of mounting 528-pin surface-mounted PGA

Photo 1-6 shows the appearance of the 528-pin surface mount PGA.

The sample to be evaluated in this experiment was a 528-pin ceramic PGA with heat sink, which is employed in large mainframe computers.

In this experiment, the "screen thickness" and the "reflow method" were varied to perform the evaluation.

Photo 1-6. 528-Pin Surface Mount PGA

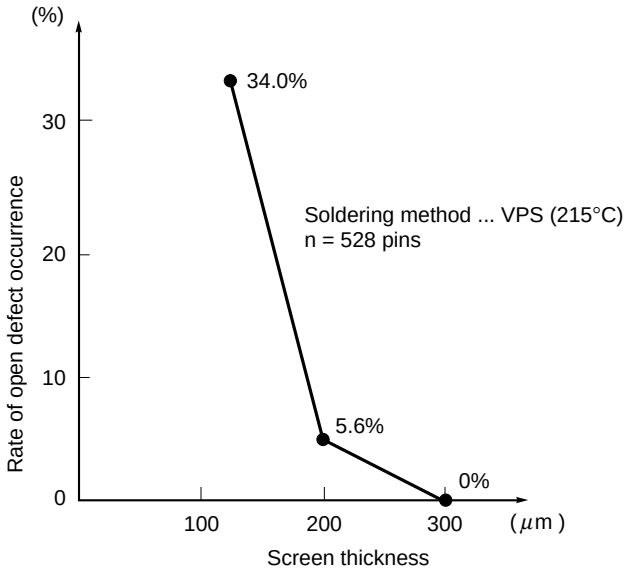


<1> Screen thickness

Figure 1-75 shows the rate of occurrence of opening when the 528-pin PGA package was mounted by means of VPS.

This figure indicates that to mount this package, a metal screen with a thickness of 300 μm is necessary.

Figure 1-75. Rate of Open Defect Occurrence with 528-pin Surface Mount PGA



<2> Reflow method

Three reflow methods were tried: hot air reflow, hot air and infrared reflow (hot air + IR), and vapor phase reflow (VPS).

Figure 1-76 shows the temperature profile of hot air reflow, **Figure 1-77** shows the temperature profile of hot air + IR, and **Figure 1-78** shows the temperature profile of VPS.

As shown in **Figures 1-76** and **1-77**, the pin temperature of the sample rose to only around 200°C even when the PWB surface temperature had risen to 330°C, and sufficient solderability could not be obtained (opening occurred).

Moreover, if a plastic QFP products (14 x 20 mm, t = 2.7 mm) was soldered along with the sample by means of hot air reflow (**Figure 1-76**), the package surface temperature rose to around 300°C, considerably exceeding the heat resistance of the plastic QFP products.

Figure 1-76. Temperature Profile of Hot Air Reflow

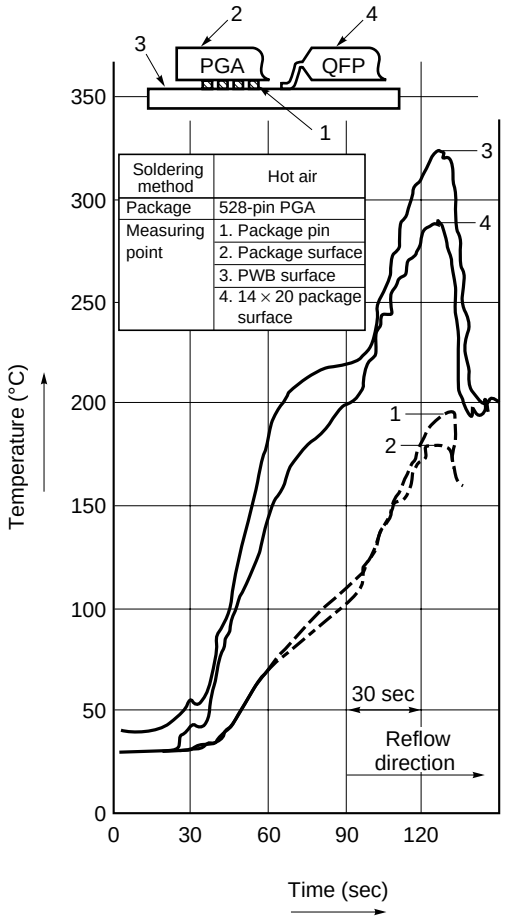
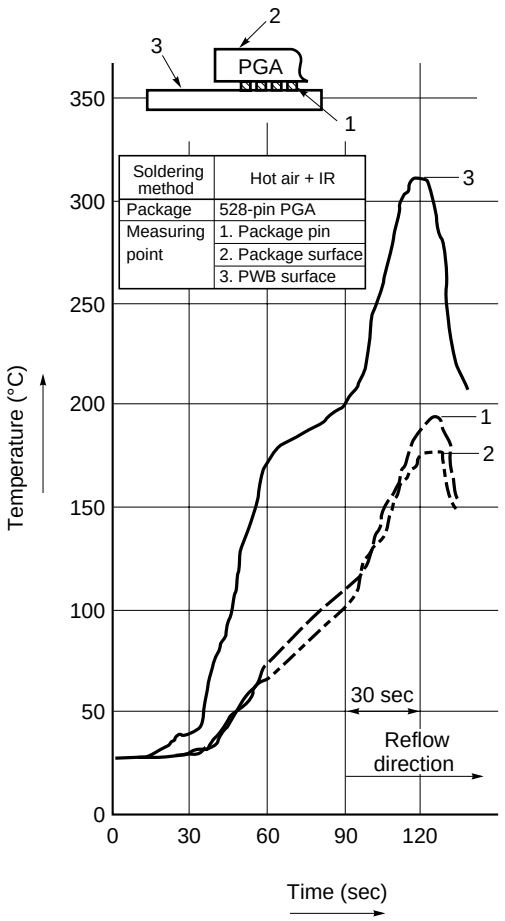


Figure 1-77. Temperature Profile of Hot Air + IR



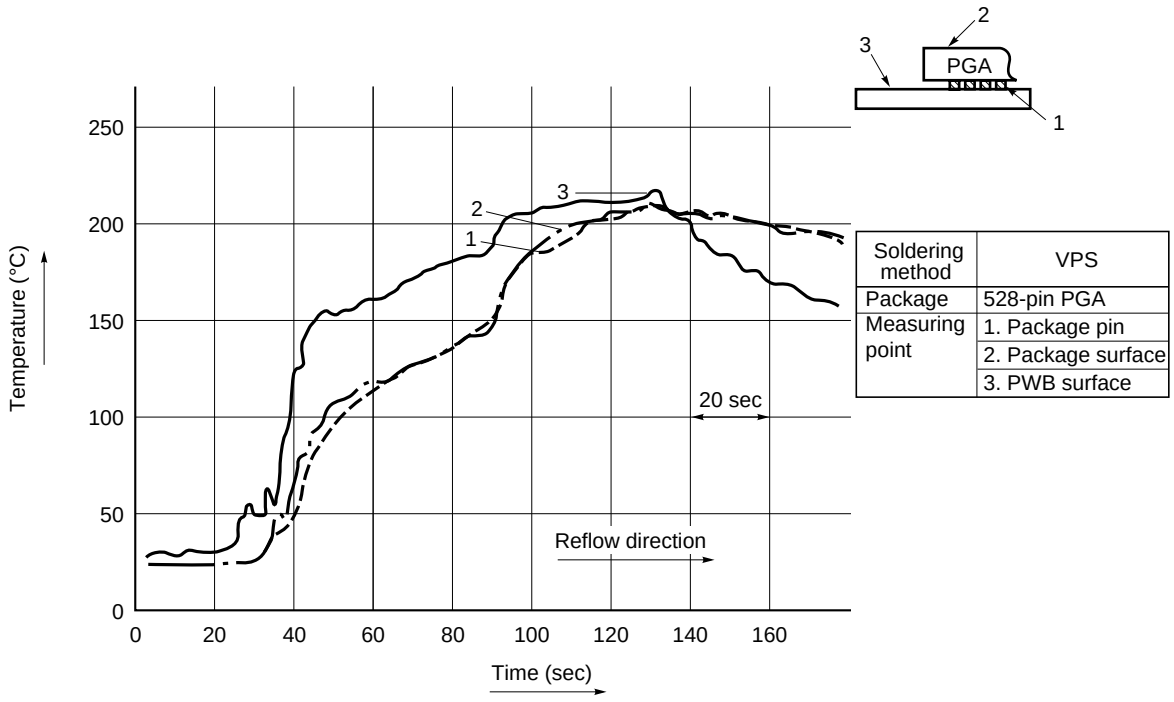
On the other hand, all the lead temperature, the surface temperature of the 528-pin PGA, and PWB surface temperature were in the vicinity of 210°C as shown in **Figure 1-78** when the sample was soldered by means of VPS, the package surface temperature did not rise so much as in the case with the hot air reflow or hot air + IR. In addition, no problem occurred even when the sample was soldered on the same PWB as a plastic QFP product.

It can therefore be concluded that the following conditions must be satisfied to obtain good solderability in soldering the 528-pin surface mount PGA package:

<<Mounting conditions of 528-pin ceramic PGA package>>

- Soldering method: VPS (215°C peak, 200°C MIN., 40 s)
- Screen thickness: 300 μm (ratio of pad area to screen opening area is 1:1)

Figure 1-78. Temperature Profile of VPS



1.5.5 Evaluation example of mounting Ball Grid Array (BGA)

The BGA is gaining popularity because it is (1) easy to handle (no lead distortion) and (2) has less mounting area. This section introduces the following BGA evaluations.

<1> Combined mounting and reflow with QFP
<2> Self-alignment effect
<3> Screen thickness
<4> Example of soldered joint temperature cycle test result
<5> Inspection after mounting
<6> Reworking BGA soldering

(1) Combined mounting with QFP and reflow

Figure 1-79 shows temperatures of each measuring point when the 225-pin BGA and QFP (14 × 20) are mounted together. This figure shows that the package surface temperature of BGA is 230˚C and QFP is 225˚C, and the bump temperature is 210˚C. This ensures good soldering ability (**Photo 1-7**).

Figure 1-79. Temperature Profile of BGA

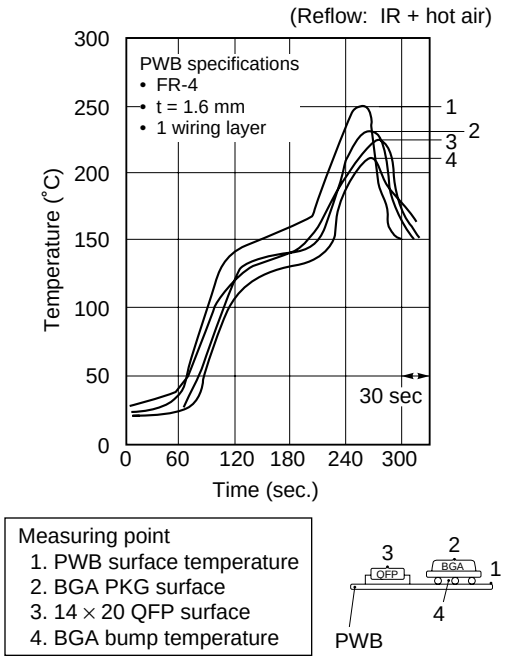


Photo 1-7. Soldering Cross-Section of BGA

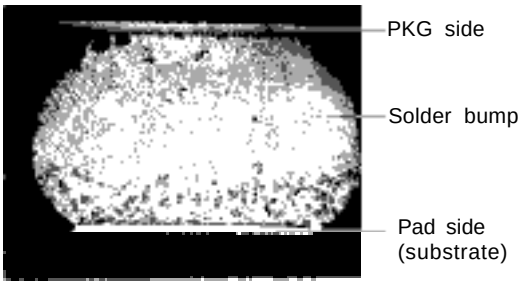
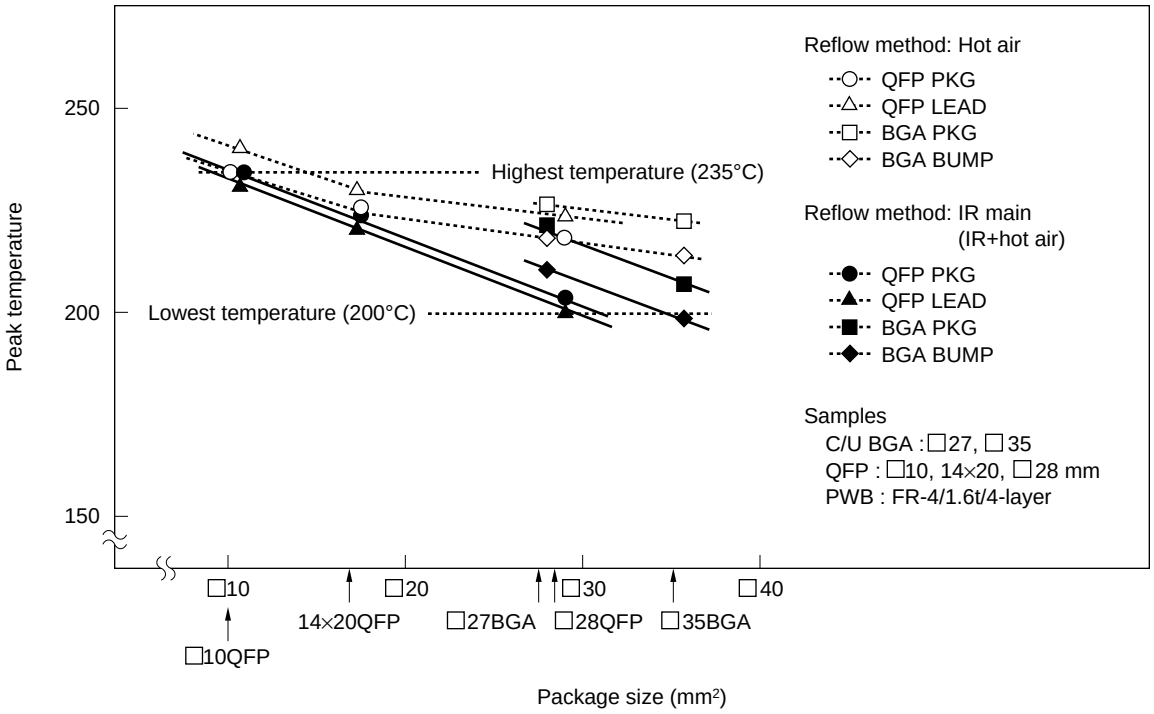


Figure 1-80 shows the relation between BGA and QFP package sizes and peak temperature when using reflow soldering.

It can be seen from **Figure 1-80** that peak temperature characteristics when using reflow soldering vary greatly. In other words, temperature dependence in relation to size is very important when using IR + hot air reflow, where IR is most important, and the possible combined mounting area in relation to the package size is small. On the other hand, when using the hot air reflow method, the possible combined mounting area in relation to the package size become extremely large.

Therefore, if implementing mounting for wide package sizes including BGAs, hot air reflow or IR + hot air reflow where hot air is most important, is recommended.

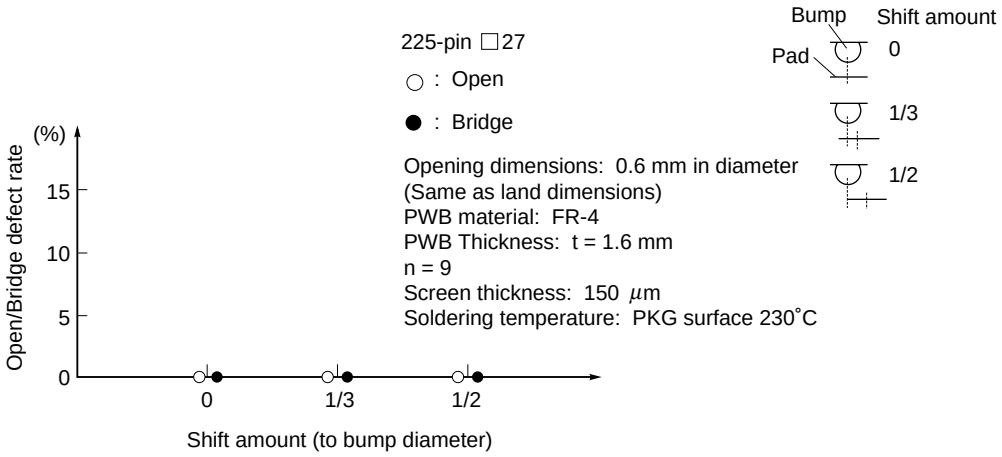
Figure 1-80. Relation between BGA and QFP Package Size and Reflow Peak Temperature (comparison of reflow methods)



(2) Self-alignment effect

Figure 1-81 shows that results of mounting a BGA package with a solder bump intentionally shifted from a mounting pad. It can be seen from this figure that the BGA package has a higher self-alignment ability.

Figure 1-81. Self-Alignment Effect



(3) Screen thickness

Table 1-23 shows the mountability of BGA packages and QFP packages according to the solder amount (screen thickness). In this evaluation, the combined-mountability of BGA and QFP is examined in consideration with the pin pitch and screen thickness of the BGA and QFP. In general, a screen thickness of 0.15 mm or less is used for a pin pitch of 0.5 mm or less, while a screen thickness of 0.15 mm to 0.20 mm is used for a pin pitch of 0.5 mm or more. This evaluation shows that the screen thickness should be selected according to the pin pitch for combined mounting of BGAs and QFPs.

Table 1-23. Mountability according to Solder Amount

(The figures in the table show the number of mounted device)

Package	BGA						QFP			
	1.27-mm pitch PBGA 225-pin		1.0-mm pitch TBGA 696-pin		0.8-mm pitch FPBGA 116-pin		0.5-mm pitch 208-pin		0.4-mm pitch 256-pin	
Opening width	ϕ0.6		ϕ0.5		ϕ0.35		0.25 x 1.4		0.20 x 1.4	
Screen thickness	Open	Bridge	Open	Bridge	Open	Bridge	Open	Bridge	Open	Bridge
100 μm	0/200	0/200	0/180	0/180	0/100	0/100	2/100	0/100	4/10	0/100
120 μm	0/200	0/200	0/180	0/180	0/100	0/100	0/100	0/100	0/10	0/100
150 μm	0/200	0/200	0/180	0/180	0/100	0/100	0/100	0/100	0/10	0/100
200 μm	0/200	0/200	0/180	0/180	Cannot be printed	Cannot be printed	0/100	0/100	Cannot be printed	Cannot be printed

(4) Example of soldered joint temperature cycle test result

Table 1-24 shows an example of evaluation of soldered joint, where various BGAs are soldered to an FR-4 PWB, using the temperature cycle test.

The results indicate that BGA soldered joints have good reliability.

Table 1-24. Result of Soldered Joint Temperature Cycle Test (Example)

	Temperature cycle conditions (˚C)	No. of samples (unit)	No. of temperature cycles					Mounting conditions
			0	300	600	700	1000	
PBGA	–40/125	17	0	0	0	0	0	A
	–65/125	17	0	0	0	0	0	
TBGA	–40/125	15	0	0	0	0	0	
	–65/125	15	0	0	0	0	0	
FBGA 0.8 mm	–40/125	15	0	0	0	—	—	B
	–65/125	15	0	0	0	—	—	

Mounting condition A:

BGA : PBGA 27 x 27 mm, 225-pin
TBGA 40 x 40 mm, 576-pin
PWB : Material/thickness : FR-4/1.6 mm
Specification: Double-sided/2-layer
Land diameter: ϕ0.6 mm
Land type: No resist overlap
Land surface process: Preflux only/no Au plating
Mounting conditions: Screen thickness/opening width : 150 μm/ϕ0.6 mm
Bump temperature: 215˚C
Reflow method: IR + AIR

Mounting condition B:

BGA : FPBGA 12 x 12 mm, 116-pin
PWB : Material/thickness : FR-4/0.8 mm
Specification: Build-up PWB/4-layer
Land diameter: ϕ0.35 mm
Land type: No resist overlap
Land surface process: Preflux only/no Au plating
Mounting conditions: Screen thickness/opening width : 150 μm/ϕ0.35 mm
Bump temperature: 215˚C
Reflow method: IR + AIR

(5) Inspection after mounting

Two methods are generally used in inspections after mounting BGA packages. One is a method to inspect the joint of a solder ball and a PWB by examining the size of the shadow of a solder ball using an X-ray inspection equipment, and the other is a method to perform electrical inspection through tester check. The following shows inspection examples.

X-ray inspection method

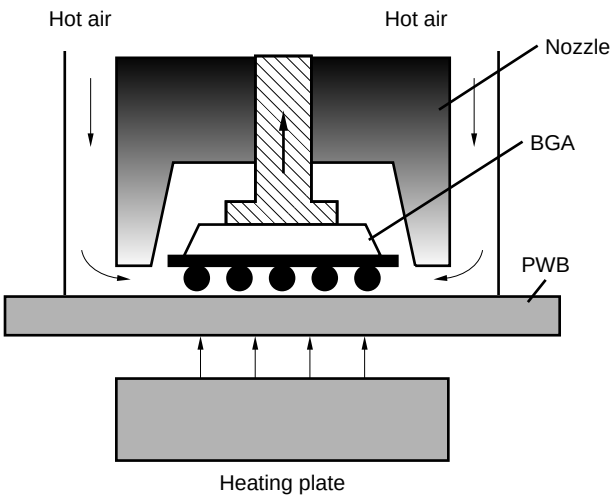
- Manufacturer: 4pi Systems, type name: 5DX, 3DX
  Nicolet, type name: CXI3800, MV6000

Electrical inspection method

1. JTAG (Joint Test Action Group) = Boundary scan/IEEE standard
2. All-pin electrical check
   Draws out the wiring of all the pins from a mounting pad, and performs electrical check by setting up a probe.

(6) Reworking BGA soldering

Rework BGAs in the process and with the reworking equipment that are shown below.



Process:

1. Heat the unsuccessfully soldered BGA with hot air, and remove it.
2. Remove residual solder on the PWB.
3. Put solder paste onto the PWB in screen printing method using self-prepared jigs. (Appropriate screen thickness is about 150 μm.)
4. Put a new BGA on the PWB so that each BGA ball and PWB land match, by observing with a monitor.

Reworking equipment:

HG7900 (manufactured by M&M Products Corp.)

Reworking of various BGA packages is enabled with the reworking equipment shown above.

Implementation example:

Working conditions for various BGA packages are described in **APPENDIX** for reference.

In the case of actual reworking, if the PWB and other parts are used in mix mass production, checking the work conditions is recommended.

1.5.6 Evaluation examples related to cleaning and non-cleaning

(1) Evaluation examples of cleaning solvents

An experiment was conducted to test the moisture proofness (PCT) of SMDs with 12 types of cleaning solvents that do not damage the ozone layer (including Bioact EC-7, P3 Cold Cleaner 375, Clean Through 710M, and Pinealpha ST-100S). **Tables 1-25** and **1-26** show the result of the experiment.

No defect occurred with any of the sample SMDs that had already been cleaned with each cleaning solvent, and no superiority in PCT was observed when these samples were compared with the reference (non-cleaned sample). It is therefore concluded that any cleaning solvent can be used as long as the soldering conditions and cleaning conditions recommended by NEC are satisfied.

Use of fleon-based solvents Fleon TES and AK-225AES, and chlorine-based solvent Ethana VG is not recommended because these solvents may damage and contaminate environments.

Table 1-25. Result of Evaluating Resistance to Cleaning Solvents 1

	Cleaning solvent	Cleaning condition	PCT evaluation result (125°C, 2.3 atm, 100% RH)			
			μPD421000LA (26-pin SOJ)	μPD65050GF (100-pin QFP)	μPC4558G2 (8-pin SOP)	μPD74HC190GS (16-pin SOP)
1	Fleon TES	Series	0/20	0/20	0/20	0/20
		Rinse	0/20	0/20	0/20	0/20
2	Ethana VG	Series	0/20	0/20	0/20	0/20
		Rinse	0/20	0/20	0/20	0/20
3	I.P.A	Rinse	0/20	0/20	0/20	0/20
4	Xylene	Rinse	0/20	0/20	0/20	0/20
5	Bioact EC-7	Rinse	0/20	0/20	0/20	0/20
6	Orenco 6000	Rinse	0/20	0/20	0/20	0/20
7	Saltol 2110	Rinse	0/20	0/20	0/20	0/20
8	Reference	—	0/20	0/20	0/20	0/20

Note Series cleaning: Ultrasonic (3 minutes) → dipping (3 minutes) → vapor (3 minutes)
Rinsing: At room temperature for 3 minutes (rinsing with tap water for 10 minutes with Bioact EC-7, Orenco 6000, and Saltol 2110)
Evaluation conditions: Moisture absorption preprocess → heating process (IR + hot air reflow) → cleaning process → PCT
PCT time: 192 hours: μPD421000LA, μPD65050GF
100 hours: μPC4558G2
96 hours: μPD74HC190GS

Table 1-26. Result of Evaluating Resistance to Cleaning Solvents 2

	Cleaning solvent	Cleaning condition	PCT evaluation result (125°C, 2.3 atm, 100% RH)			
			μPD7228AG* (80-pin QFP)	μPD43256AGX* (32-pin TSOP)	μPD65081GF* (80-pin QFP)	μPC4558G2** (8-pin SOP)
1	P3 Cold Cleaner 375	Ultrasonic cleaning ↓ rinse	0/20	0/20	0/20	0/20
2	Clean Through 710M		0/20	0/20	0/20	0/20
3	Pinealpha ST-100S		0/20	0/20	0/20	0/20
4	Acsarel R32		0/20	0/20	0/20	0/20
5	AK-225AES		0/20	0/20	0/20	0/20
6	Reference	—	0/20	0/20	0/20	0/20

Note Cleaning conditions: Ultrasonic cleaning for 5 minutes → rinsing with tap water for 10 minutes (no rinsing with AK-225AES)

Evaluation conditions *: Moisture absorption preprocess → heating process (IR + hot air reflow) → cleaning process → PCT

**: Moisture absorption preprocess → heating process (wave soldering) → cleaning process → PCT

PCT time: 192 hours: μPD7228AG, μPD43256AGX, μPD65081GF

100 hours: μPC4558G2

(2) Evaluation example of non-cleaning flux

Evaluation on the moisture resistance of SMDs was made when the SMDs were applied (or dipped into) five types of non-cleaning fluxes. **Tables 1-27** and **1-28** show the result of the evaluation. The samples applied or dipped into each type of flux showed no superiority in PCT or HHBT to the reference (to which the flux was not applied).

It is therefore concluded that the fluxes listed in **Table 1-25**, and fluxes with a chlorine content of 0.2 wt% or less can be used without cleaning, as long as the sample is subject to the thermal stress within the range recommended by NEC.

However, it is assumed that influences of flux residues on the PWB on which the components have been already mounted, and semiconductor devices vary because many types of fluxes are actually used with different soldering methods.

In addition, flux residues may absorb moisture, helping migration of tin and silver.

It is therefore important that a thorough evaluation be made with an appropriate PWB to confirm that no problem occurs even if cleaning is not performed after the devices have been mounted with a particular flux.

Table 1-27. Result of Evaluating Resistance to Flux 1

	Flux type	Chlorine content (wt%)	PCT evaluation result (125°C, 2.3 atm, 100% RH)			
			μPD421000LA (26-pin SOJ)	μPD65013GF (100-pin QFP)	μPC4558G2 (8-pin SOP)	μPD74HC190GS (16-pin SOP)
1	Rapix RMA	0	0/20	0/20	0/20	0/20
2	Reference	—	0/20	0/20	0/20	0/20

Note Flux application: Applied with thin brush to all pins at base
Evaluation conditions: Moisture absorption preprocess → flux application → heating process (IR + hot air reflow) → PCT
PCT time: 192 hours : μPD421000LA, μPD65013GF
100 hours : μPC4558G2
96 hours : μPD74HC190GS

Table 1-28. Result of Evaluating Resistance to Flux 2

	Flux type	Chlorine content (wt%)	HHBT evaluation result (85°C, 85% RH, rated bias)			
			μPD43256AGU (28-pin SOP)	μPD7514G (80-pin QFP)	μPC65240GD (160-pin SOP)	μPC451G2 (14-pin SOP)
1	ULF-500VS	0.04	0/20	0/20	0/20	0/20
2	ULF-210R	0	0/20	0/20	0/20	0/20
3	CF-220V	0.09	0/20	0/20	0/20	0/20
4	AM-173	0.2	0/20	0/20	0/20	0/20
5	Reference	—	0/20	0/20	0/20	0/20

Note Evaluation conditions: Moisture absorption preprocess → heating process (IR) → immersion in flux → dry → HHBT
HHBT time: 1500 hours: μPD43256AGU
2000 hours: μPD7514G, μPD65240GD, μPC451G2

1.6 SMD Reliability Data

This section describes the outline of moisture resistance tests conducted after SMDs have been soldered, and examples of the test results.

1.6.1 Outline of moisture resistance test

Here is an example of a moisture resistance test (compound test) conducted by NEC to determine the recommended SMD soldering conditions:

Preprocess (mainly applied to IC products)		Solder heat		Reliability test
Moisture absorption by HH (85°C, 85% RH), or moisture absorption by HH (30°C, 70% RH)	→	IR reflow or VPS reflow or wave soldering	→	No defect at 1000 hours after HHBT (85°C, 85% RH, with rated bias applied), or no defect at 192 hours after PCT (125°C, 2.3 atm)

<Preprocess>

- The standard for the product for which moisture absorption control is not necessary is equivalent to saturated moisture absorption at 30°C, 85% RH (on the assumption that the products are used in a high-temperature and humidity region). However, since moisture absorption at 30°C, 85% RH takes a long time, the actual test is conducted under accelerated conditions of 85°C, 85% RH (the moisture absorption time differs depending on the thickness of the package and other factors).
- The standard for the product for which moisture absorption control is necessary is at 30°C, 70% RH (the moisture absorption time differs depending on the product).

<Solder heat>

- The resistance of NEC's SMDs to soldering heat is evaluated by imposing a thermal stress to the SMDs with any of the soldering methods listed above. The thermal stress is imposed one, two, or three times with the temperature profile shown in **Figures 1-58** to **1-61** if the soldering method is infrared or VPS reflow soldering. Wave soldering is performed under the conditions shown in **Table 1-20**.
  Some products, however, are evaluated with the thermal stress applied one, two, or three times with the temperature profile shown in **Figure 1-58** to **Figure 1-61** when infrared reflow soldering is used.

<Reliability test>

- NEC basically conducts HHBT and PCT tests described above to check the moisture resistance of its SMDs after they have been soldered.
- The resistive time of some products may be 192 hours or less in the case of the PCT test. Moreover, the PCT test is conducted as a reference test for some products.

1.6.2 Result of moisture resistance test

This section shows the results of moisture resistance test conducted on NEC's representative products in accordance with the method mentioned in the preceding section.

As described in section **1.4**, NEC's recommended soldering conditions are specified for each product, not for a group of packages or products.

For reference, a symbol code indicating a recommended soldering conditions is shown in the column right to that indicating the test result. (For details on the meanings of these codes, refer to paragraph **(3)** in section **1.4.1**. These codes are used as of 1996.)

Note The "preprocess conditions" in the following table are as follows:
HH1 ... stored at 85°C, 85% RH, for 48 hours (moisture absorption processing)
HH2 ... stored at 85°C, 85% RH, for 144 hours (moisture absorption processing)
HH3 ... stored at 30°C, 70% RH, for 178 hours (moisture absorption processing)
HH4 ... stored at 85°C, 85% RH, for 24 hours (moisture absorption processing)

(1) Result of moisture resistance test of IC products

(a) Example of test result of SOP

<1> μPD4991AGS (20-pin, 300 mil SOP, real-time clock)

Soldering process	Preprocess conditions	Test item	Test conditions	Test result	Symbol code
IR reflow, 3 times (**Figure 1-58**)	HH1	High-temperature, high-humidity bias (HHBT)	T_a = 85°C, RH = 85%, applied 7 V, t = 1000 H	0/20	IR35-00-3
		PCT	T_a = 125°C, RH = 100%, 2.3 atm, t = 192 H	0/20	

<2> μPD74HC00GS (14-pin, 300 mil SOP, CMOS high-speed logic)

Soldering process	Preprocess conditions	Test item	Test conditions	Test result	Symbol code
IR reflow, 3 times (**Figure 1-58**)	HH1	High-temperature, high-humidity bias (HHBT)	T_a = 85°C, RH = 85%, applied 7 V, t = 1000 H	0/22	IR35-00-3
		PCT	T_a = 125°C, RH = 100%, 2.3 atm, t = 192 H	0/22	

(b) Example of test result of QFP

<1> μPD65841GK (80-pin QFP, 1.05 mm thick, CMOS gate array)

Soldering process	Preprocess conditions	Test item	Test conditions	Test result	Symbol code
IR reflow, 3 times (**Figure 1-58**)	HH3	High-temperature, high-humidity bias (HHBT)	T_a = 85°C, RH = 85%, applied 3.6 V, t = 1000 H	0/24	IR35-107-3
		PCT	T_a = 125°C, RH = 100%, 2.3 atm, t = 192 H	0/20	

<2> μPD65843GC (100-pin QFP, 1.45 mm thick, CMOS gate array)

Soldering process	Preprocess conditions	Test item		Test result	Symbol code
IR reflow, 3 times (**Figure 1-58**)	HH3	High-temperature, high-humidity bias (HHBT)		0/24	IR35-107-3
		PCT		0/20	

<3> μPD65806GM (160-pin QFP, 2.7 mm thick, CMOS gate array)

Soldering process	Preprocess conditions	Test item	Test conditions	Test result	Symbol code
IR reflow, 3 times (**Figure 1-58**)	HH2	High-temperature, high-humidity bias (HHBT)	T_a = 85°C, RH = 85%, applied 5.5 V, t = 1000 H	0/24	IR35-00-3
		PCT	T_a = 125°C, RH = 100%, 2.3 atm, t = 192 H	0/20	

(c) Examples of test results of SOJ

<1> μPD421805LE (28-pin SOJ, 4M dynamic RAM)

Soldering process	Preprocess conditions	Test item	Test conditions	Test result	Symbol code
IR reflow, 3 times (**Figure 1-58**)	HH3	High-temperature, high-humidity bias (HHBT)	T_a = 85°C, RH = 85%, applied 5.5 V, t = 1000 H	0/135	IR35-207-3
		PCT	T_a = 125°C, RH = 100%, 2.3 atm, t = 192 H	0/66	

<2> μPD4216160/4216165LE (42-pin SOJ, 16M dynamic RAM)

Soldering process	Preprocess conditions	Test item	Test conditions	Test result	Symbol code
IR reflow, 3 times (**Figure 1-58**)	HH3	High-temperature, high-humidity bias (HHBT)	T_a = 85°C, RH = 85%, applied 5.5 V, t = 1000 H	0/153	IR35-207-3
		PCT	T_a = 125°C, RH = 100%, 2.3 atm, t = 192 H	0/351	

(2) Results of moisture resistance test of discrete devices

(a) Example of test result of MP-2

<1> 2SJ462 (MP-2, silicon transistor)

Soldering process	Preprocess conditions	Test item	Test conditions	Test result	Symbol code
IR reflow, 3 times (**Figure 1-58**)	HH4	High-temperature, high-humidity bias (HHBT)	T_a = 85°C, RH = 85%, applied 30 V, t = 1000 H	0/20	IR35-00-3
		PCT	T_a = 125°C, RH = 100%, 2.3 atm, t = 200 H	0/20	

(b) Example of test result of power mini-mold

<1> 2SK2159 (power mini-mold (SC-62), silicon transistor)

Soldering process	Preprocess conditions	Test item	Test conditions	Test result	Symbol code
IR reflow, 3 times (**Figure 1-58**)	HH4	High-temperature, high-humidity bias (HHBT)	T_a = 85°C, RH = 85%, applied 30 V, t = 1000 H	0/20	IR35-00-3
		PCT	T_a = 125°C, RH = 100%, 2.3 atm, t = 200 H	0/20	

(c) Example of test result of small mini-mold

<1> 2SK2090 (small mini-mold (SC-70), silicon transistor)

Soldering process	Preprocess conditions	Test item	Test conditions	Test result	Symbol code
IR reflow, 3 times (**Figure 1-58**)	HH4	High-temperature, high-humidity bias (HHBT)	T_a = 85°C, RH = 85%, applied 30 V, t = 1000 H	0/20	IR35-00-3
		PCT	T_a = 125°C, RH = 100%, 2.3 atm, t = 200 H	0/20	

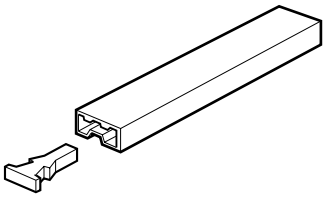
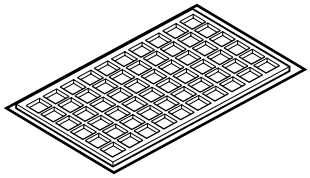
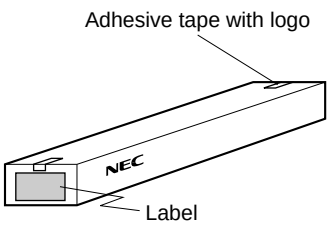
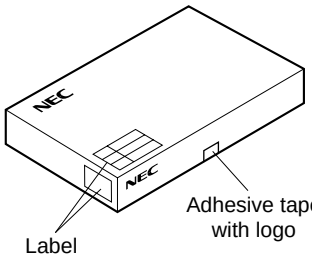
1.7 Packing

1.7.1 Packing style and notes

(1) Packing style of IC products

Table 1-29 shows the general packing styles of NEC's SMDs.

Table 1-29. Packing Styles of SMDs

	Magazine	Tray	Tape
Individual packing container			
Individual packing box			

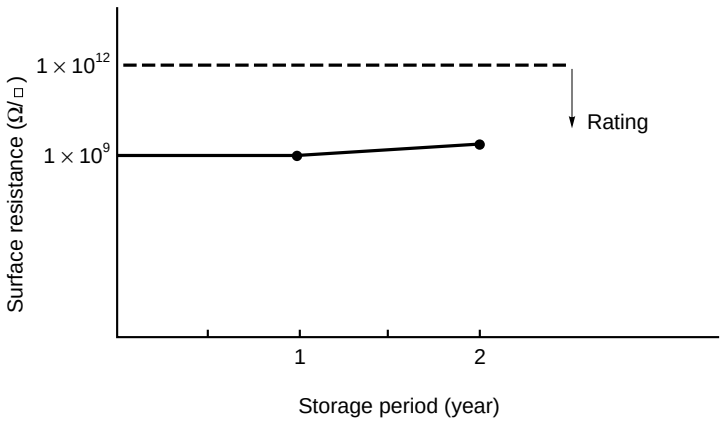
(2) Notes on handling

(a) Exercise care in handling the interior box.
If excessive shock or vibration is applied to the SMD while transported, the pins of the SMD may be deformed, or the SMD itself may be damaged. Pay special attention especially after they are taken from their individual box. If SMDs placed together in a bag or fixed on a tray fall on the ground, pins of the SMDs or the tray can be deformed or damaged by the shock.
Avoid location where the temperature and humidity are high to store the SMD.

(b) Packing materials of IC (tray, magazine, etc.) are implemented with anti-static measures. However, exercise care against static electricity in handling products.

(c) Bear in mind the following points in handling the transparent plastic magazine case as it is applied anti-static agent on the surface:
<1> If the case is cleaned with water, the anti-static agent dissolves in water, and the anti-static effect may be lost.
<2> If the surface of the case is rubbed many times, the anti-static effect may be degraded. Do not frequently put or take out the SMDs into or out of the case.
Under the normal storage conditions, the surface resistance of the case does not age as shown in **Figure 1-82**, satisfying the ratings of 1.0×10^{12} MAX. (Ω/□) specified by NEC.

Figure 1-82. Aging of Surface Resistance of Magazine Case



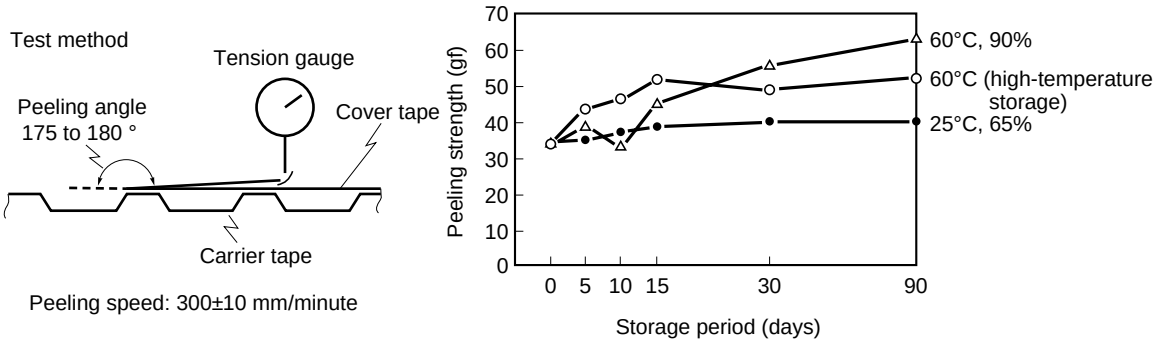
(d) Storage
If the storage environments are exceptionally poor, solderability may be degraded, the appearance may be deformed, and characteristics may be degraded.
The recommended storage conditions are as follows:
<1> Temperature : 5 to 35°C (25°C or below after opening dry pack)
<2> Humidity : 45 to 75% RH (65% RH or less after opening dry pack)
<3> Atmosphere : Must be free from toxic gas such as sulfur dioxide and not dusty.
<4> Others : Must be free from vibration and shock that may deform the packing container. Be careful not to apply too much weight to packing containers when piling them. If more than two years have elapsed since the date of manufacture, it is recommended to verify the solderability and to check the rust on the pins before using the product.

(e) Peeling strength of embossed sealing tape

The peeling strength of NEC's embossed sealing tape is 10 to 70 gf under the normal storage conditions (**Figure 1-83**).

Take this into consideration if the SMDs are supplied from the embossed taping to the mounting machine.

Figure 1-83. Peeling Strength of Embossed Tape



(f) Handling tray

To avoid bending of the leads resulting from the improper placement of stored ICs on trap, exercise care about the following points.

<1> Hold the tray firmly when cutting the bundle tape.

<2> Do not move the tray while it is not bundled.

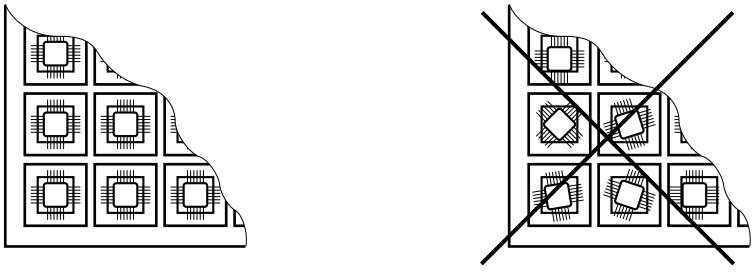
<3> When replacing the products in the tray, exercise care that the leads of the products are not bent (use of a vacuum forceps or absorber is recommended to prevent touching the leads).

<4> Make sure that the products are stored in the correct positions on the tray (**Figure 1-84**).

<5> Do not apply shocks to the trays when piling up trays.

<6> If an IC is improperly placed, the space between its tray and the tray placed avobe it becomes wider. Ensure that the spaces between trays are all the same.

Figure 1-84. Storage Positions on Tray



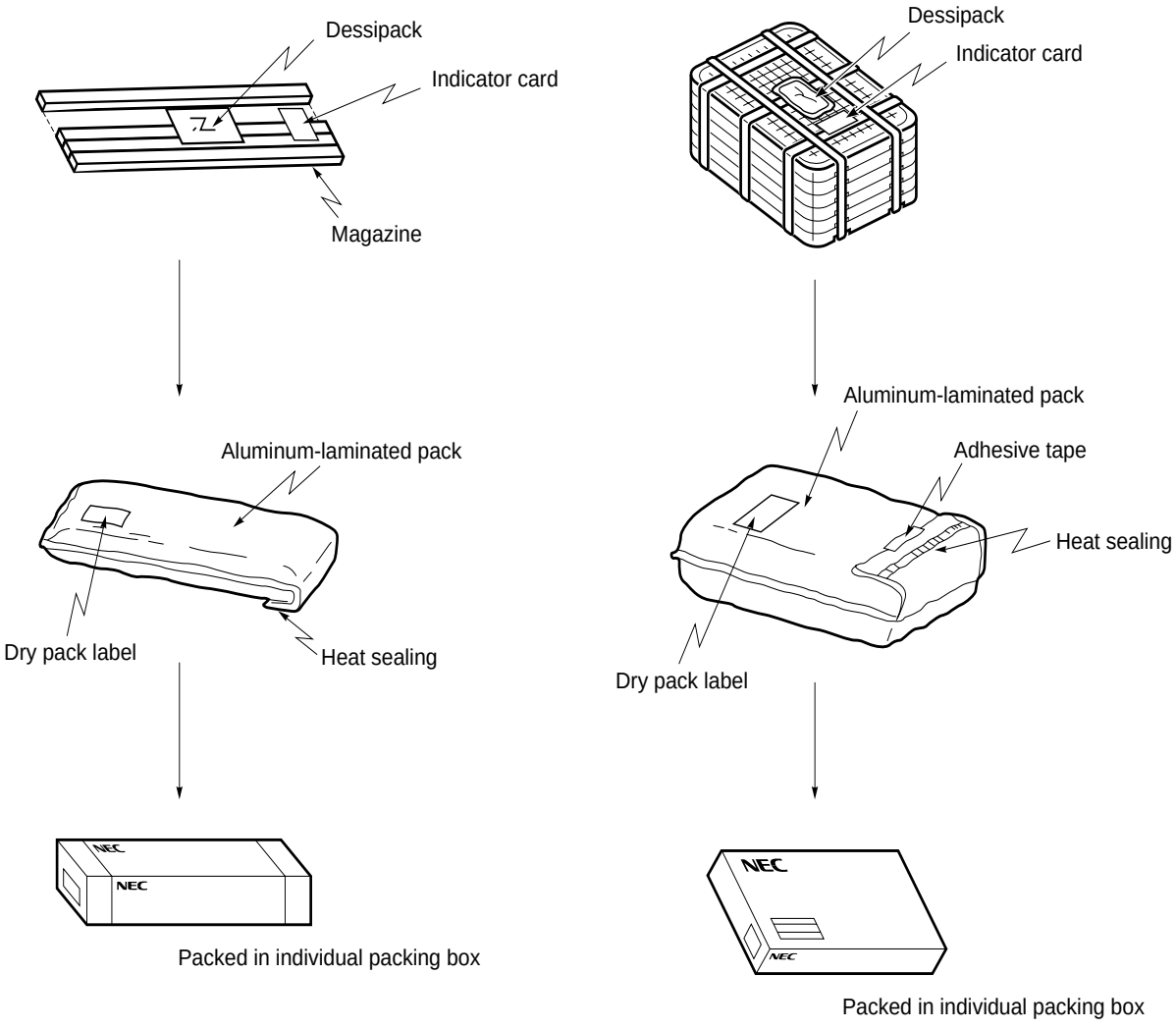
1.7.2 Dry pack and notes

(1) Dry pack

NEC used an aluminum laminated dry pack for shipment of products for which moisture absorption control is necessary before soldering, or products that are to be soldered by partial heating method.

Figure 1-85 shows the specifications of the dry pack.

Figure 1-85. Dry Pack Packing



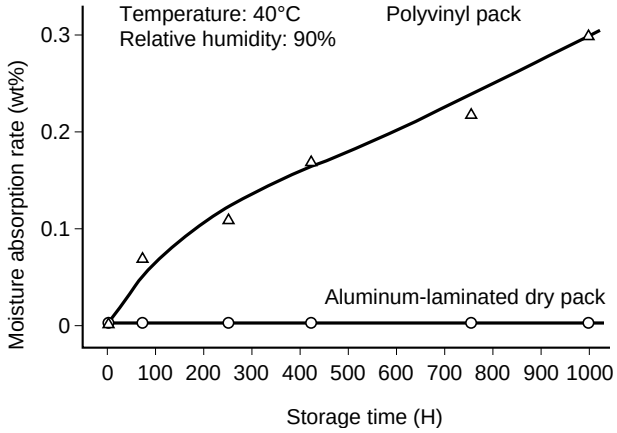
(2) Moisture absorption characteristics of dry pack

(a) Comparison between aluminum-laminated dry pack and polyvinyl pack

Figure 1-86 shows the moisture absorption characteristics of an aluminum-laminated pack and polyvinyl pack. Both the packs contain thin QFPs (1.5 mm thick) and drying agent, and are sealed by means of thermocompression. The moisture absorption characteristics are measured at an ambient temperature (T_a) of 40°C and a relative humidity (RH) of 90%.

As shown in this figure, the polyvinyl pack absorbs a fairy amount of moisture, but the aluminum-laminated pack does not at all.

Figure 1-86. Moisture Absorption Characteristics of Aluminum-Laminated/Polyvinyl Packs (package thickness: 1.5 mm)

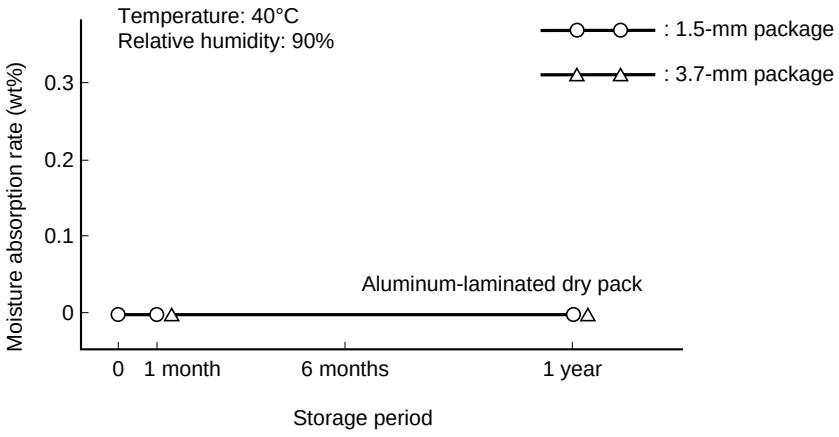


(b) 1-year storage characteristics of aluminum-laminated dry pack

Figure 1-87 shows the moisture absorption characteristics of three aluminum-laminated dry packs each containing thin and thick QFPs (1.5 mm and 3.7 mm) and a drying agent. These bags are stored in an oven at an ambient temperature (T_a) of 40°C and a relative humidity (RH) of 90% for 0 hour, 1 month, and 1 year, respectively.

This figure indicates that even the pack stored for 1 year does not absorb moisture at all, and that the aluminum-laminated packs have a complete moisture proofness.

Figure 1-87. Storage Characteristics of Aluminum-Laminated Dry Packs



(3) Notes on products packed in dry pack

<1> Exercise extreme care in handling dry packs. Do not apply excessive pressure to dry packs nor stab the dry pack with a sharp object, because this may result in damage to packing material.

<2> The dry pack contains a desiccating pack and a paper humidity indicator.
When the indicator absorbs moisture, the blue part of the indicator turns pink. (The dry pack of some products has a silica gel bag containing a blue indicator that turns pink or transparent when moisture is absorbed.)
Therefore, if the indicator has already turned pink when the dry pack is opened (if the 40% RH section has already turned pink in the case of the paper indicator), the ICs or LSIs contained in the dry pack may have absorbed moisture that has been let in due to damage to the dry pack, etc. In this case, bake the ICs or LSIs by storing them at a high temperature. Note that the baking conditions differ depending on the product. Either refer to the Data Sheet of the product, or consult NEC.

<3> Baking
After opening the dry pack, solder the products within the valid storage period specified on the label on the dry pack. If the storage period has expired, the products must be baked by storing at a high temperature.
Note that the baking conditions differ depending on the product. The conditions specified for each product must be satisfied.

<4> Heat resistance of packing materials

a) Tray
Two types of trays are available: non-heat resistive type and heat resistive type. To perform baking, use the heat resistive type.
Aluminum-laminated dry packs use heat resistive trays. “HEAT PROOF” is marked on heat resistive trays.
The maximum allowable temperature for the heat resistive type is 135˚C.
The maximum allowable temperature for non-heat resistive trays is 50˚C. Therefore, non-heat resistive trays cannot be baked.

b) Magazine case
The plastic magazine case is not heat resistive.
If baking the products contained in the plastic magazine case is unavoidable, put the products in a heat resistive container.

c) Taping
Adhesive tape and embossed tape are not heat resistive.
If baking the products packaged with these tapes is unavoidable, place the products in a heat resistive container (in this case, however, tape mounting is not possible).

Note To perform baking, be careful not to bend the leads of the products.

(4) Moisture absorption characteristics of aluminum-laminated dry pack temporarily sealed

Figure 1-88 shows the moisture absorption characteristics of an aluminum-laminated dry pack containing drying agent and thin QFPs (1.5 mm thick) that has been once opened and closed with an adhesive tape as shown in **Figure 1-89**, and stored at an ambient temperature (T_a) of 40°C and a relative humidity (RH) of 90%.

Figure 1-88 indicates that a considerable moisture proofness can be improved by temporarily closing the dry pack that has been opened once.

However, this effect is degraded if the temperature and humidity rise, and the products contained in this pack should be processed within 168 hours.

Therefore, keep in mind the following points when closing the dry pack that has been opened once with adhesive tape or similar materials:

<1> After the dry pack has been opened once, close the dry pack with an adhesive tape as shown in **Figure 1-89** within the specified valid period. Note that this can be done only once.

<2> If the dry pack has been opened once and closed again as described above, the products contained in the dry pack must be processed within 168 hours.

<3> The period during which the dry pack can remain closed without the products in it affected is not included in the specified valid period of the dry pack.

***** For the valid period after the dry pack has once been opened, refer to **(3)** in section **1.4.1**.

Figure 1-88. Moisture Absorption Characteristics of Temporarily Closed Aluminum-Laminated Dry Pack (package thickness: 1.5 mm)

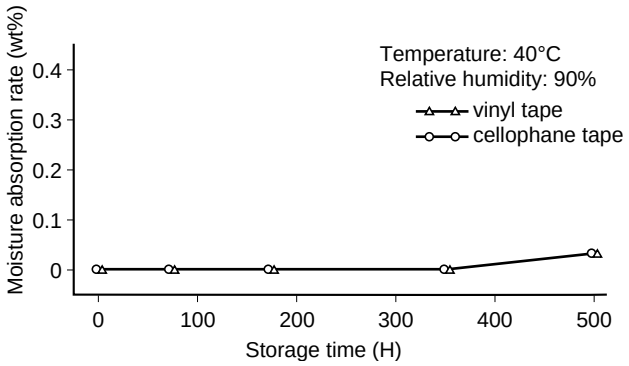
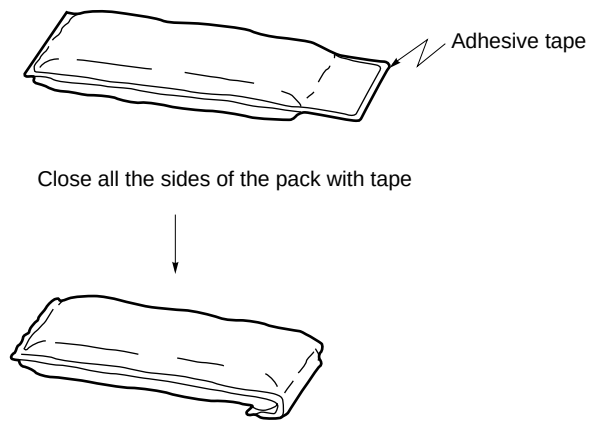
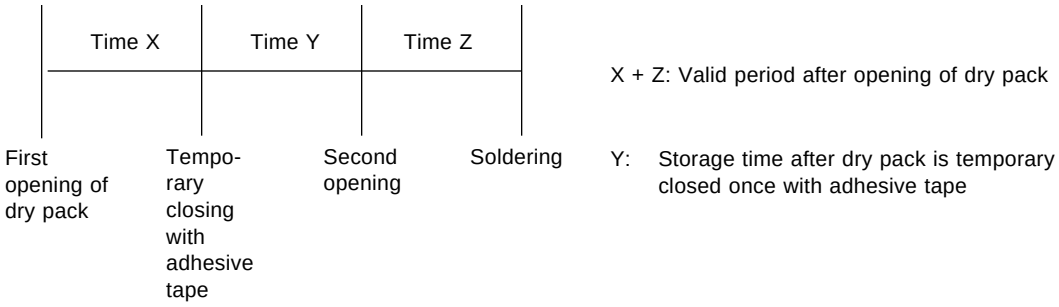


Figure 1-89. Temporarily Closing Aluminum-Laminated Dry Pack



Example) If the products are specified to be used within 72 hours after the dry pack has been opened, the valid storage period of these products is as follows:



In this case, the valid period after the dry pack has been opened once is X + Z = 72 hours, and the storage time if the dry pack is closed again with an adhesive tape Y is 168 hours. Therefore, the total storage time is 240 hours.

1.8 Handling Packages

1.8.1 Notes on use

(1) Handling packages

The pins of SMDs are easily deformed if external force is applied. In the case of an SMD with many pins, the pin at the outermost position of each side of the package is likely to be deformed.

When handling the package, therefore, do not touch the pins whenever possible. Instead, holding the package with an absorber listed in **Table 1-30** is recommended.

Table 1-30. Tools to Handle Package

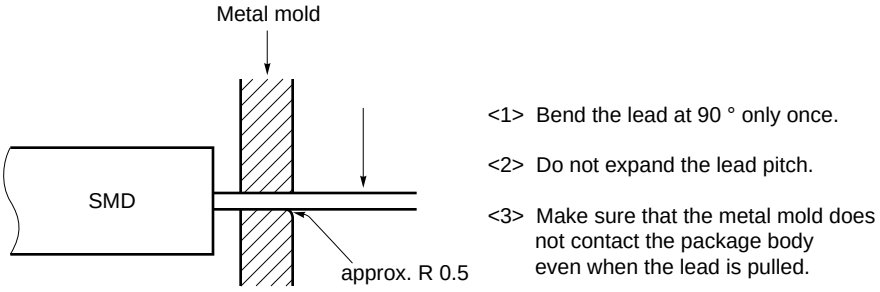
Tool	Type name	Manufacturer	Telephone number
Vacuum pen	PEN VAC	Unitecno	03 (5476) 5661

For details on each tool, consult the above manufacturer.

(2) Lead forming

To form the lead into a desired shape, securely fix the lead at the base side with pincers or a jig. When using a metal mold, make sure that a tensile force is not applied to the lead at the base side.

Figure 1-90. Forming Lead



(3) Adjustment after soldering

To make an adjustment after soldering (such as soldering unfinished, low solder quantity or difference of device locations), use of repair tools listed in **Table 1-31** is recommended. Do not use the general method (such as IR and VPS) to make an adjustment as it may cause degradation of the IC.

Table 1-31. Example of Repair Equipment

Equipment name	Type name	Manufacturer	Telephone number
SMC Hot Air Workstation	HG7900	M&M Products	03 (3274) 2431
SMT Chip Remover	SMT-2A1	OK Industries	03 (3449) 7451
Point Solder	SA-5501		

*For details on each equipment, consult its manufacturer.

(4) Infrared reflow conditions of power mini-mold and MP-3

If the power mini-mold and MP-3 type devices are soldered by directly heating them with near infrared ray, a great temperature difference occurs between the resin and heat sink. If this temperature difference exceeds 20°C, the internal bonding wire may break.

If these devices are used under the infrared reflow soldering conditions recommended by NEC satisfied, no problem occurs.

Figure 1-91 illustrates equipment for the experiment, and **Figure 1-92** shows the method to measure the temperature.

Figure 1-91. Equipment for the Experiment

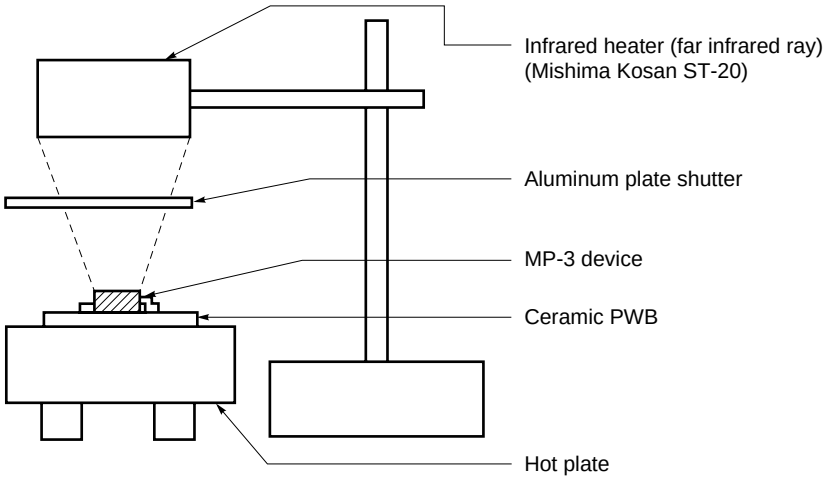
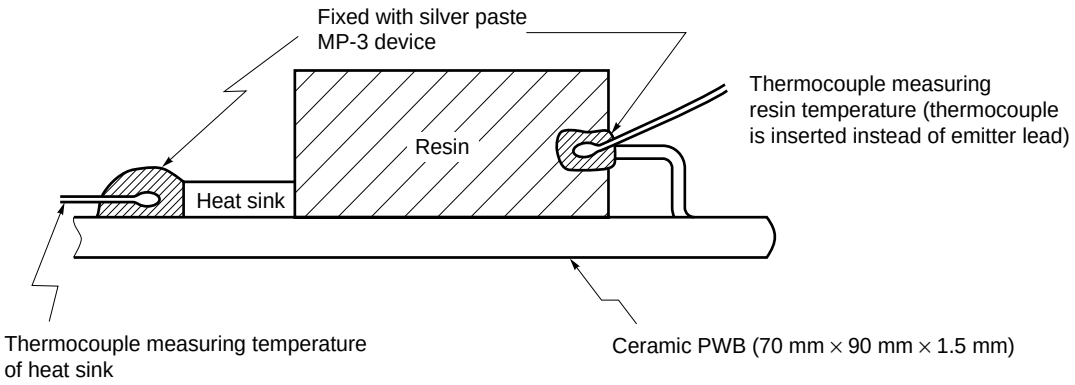


Figure 1-92. Temperature Measuring Method



(5) Exterior coating of power mini-mold and MP-3

Do not directly coat the power mini-mold and MP-3 devices with phenol resin.

Since the thermal expansion coefficient of phenol resin is different from that of the package resin and heat sink, a chip crack may occur, depending on the ambient temperature, if phenol resin is used.

If coating the device with phenol resin is unavoidable, the device must be first coated with buffer materials (such as silicon resin) as shown in **Figure 1-93**.

As a direct exterior coating material without buffer materials, rubber metamorphic phenol resin is available (example: PR-54062: Sumitomo Bakelite).

Figure 1-94 shows an example of evaluating temperature cycle resistivity when a buffer material with phenol coating and rubber metamorphic phenol resin are used.

When performing coating, evaluation according to the structure of the material is necessary.

Figure 1-93. Example of Buffer Coating

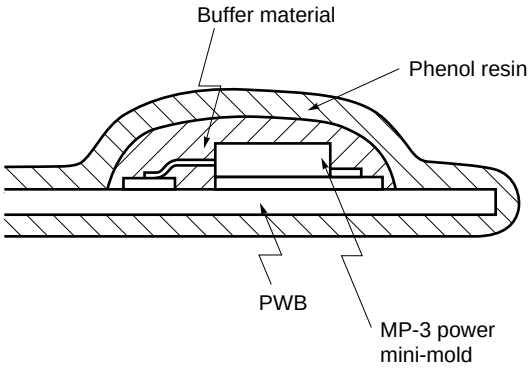
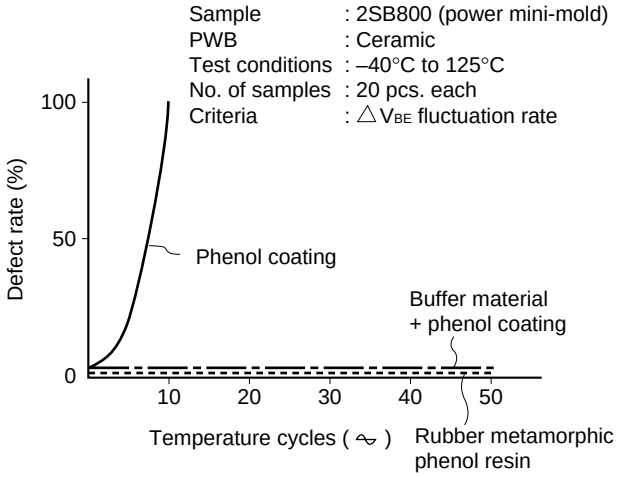


Figure 1-94. Temperature Cycle Resistivity of Phenol Coating



(6) Power dissipation of discrete device

Power dissipation P_T of a discrete device increases when the device is mounted on a PWB because of good thermal radiation, but may significantly change depending on the mounting method (size of the PWB and resin coating).

It is therefore necessary to confirm the thermal resistance of the device through a test after it has been mounted (for details, refer to NEC's technical document "Surface Mount Discrete Devices (mini-mold, power mini-mold, and MP-3" (TEM-519)).

(7) Mounting on PWB

When mounting semiconductor devices on a PWB by using a mounting machine, make sure that excessive mechanical stress is not imposed on the devices.

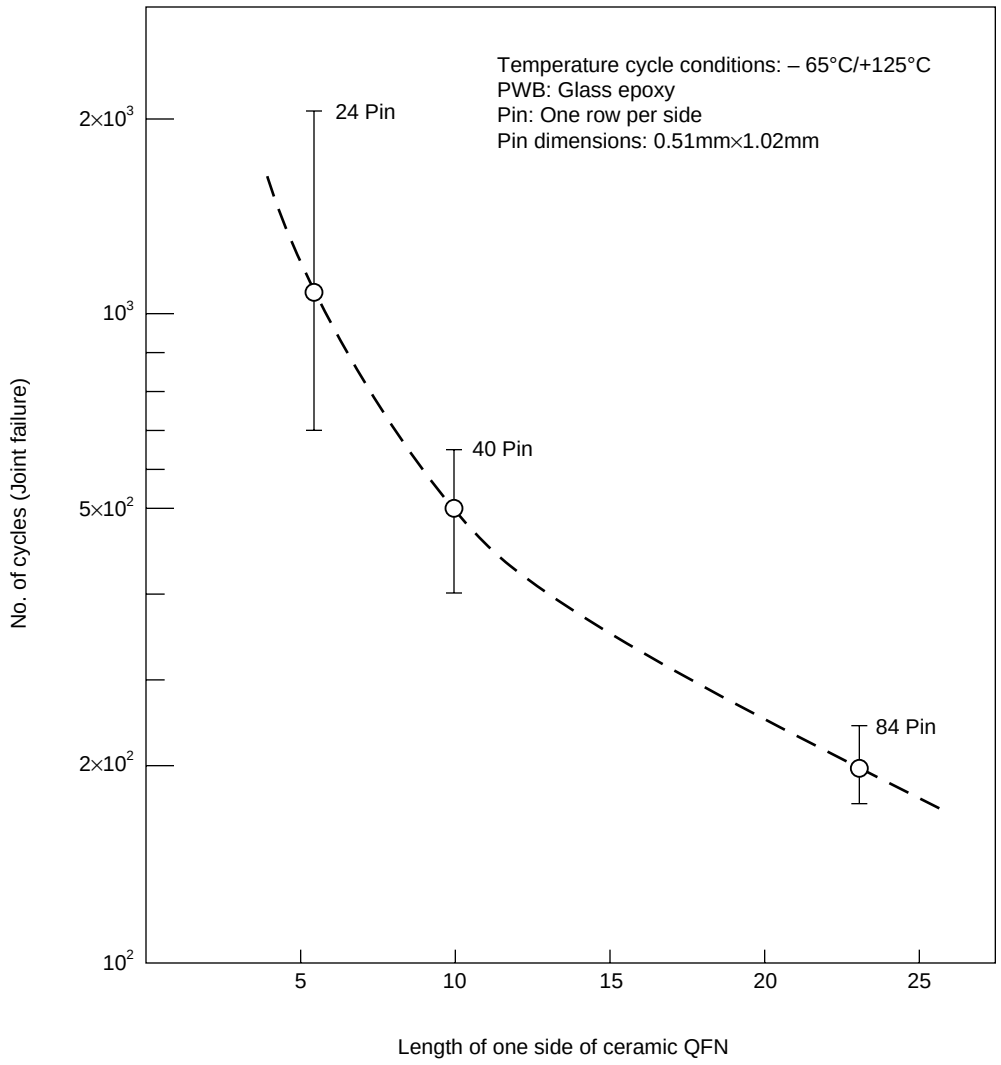
(8) Socket mounting of ceramic QFN product

Figure 1-95 shows the resistivity result to temperature cycle of soldered joint when directly soldering a ceramic QFN of a different size to a glass-epoxy board.

It can be seen from this figure that the resistivity result to temperature cycle of soldered joint worsens remarkably as the size of the ceramic QFN becomes larger.

Therefore, when mounting a ceramic QFN product of relatively large size on a plastic PWB socket mounting is recommended.

Figure 1-95. Resistivity to Temperature Cycle of QFN Package Soldered Joint



Source 1980 Electronic Communications Society National Convention
Reliability of soldered joints of multi-pin chip carriers
NTT Yoshioka et al.

1.8.2 Countermeasures against electrostatic charges

Since the packages of SMDs are generally thinner and larger in surface area than those of through-hole devices (THDs), they are likely to carry more electrostatic charges. It is therefore important:

- Not to charge the packages
- Not to place charged objects in the neighborhood of the packages
- To prevent discharging

This section describes the points to be noted from the above viewpoints.

For the problems and testing method of electrostatic discharge (ESD), refer to technical document “Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)” (C11892EJ1V0IF00).

(1) Working environment

Electrostatic charge is generated differently depending on the environments. Generally, however, the lower the relative humidity, the higher the generated voltage (refer to **Table 1-32**).

It is recommended that the relative humidity be kept whithin the range of 40 to 60 % to prevent static electricity and to limit the quantity of moisture absorbed by the packages.

Table 1-32. Example of Generation of Electrostatic Voltage

Mode of electrostatic voltage generation	Electrostatic voltage (V)	
	10 to 20% RH	65 to 90% RH
Walking on carpet	35,000	1,500
Walking on vinyl floor	12,000	250
Worker at bench	6,000	100
Vinyl cover on document	7,000	600
Polyvinyl bag picked up from bench	20,000	1,200
Working chair with polyurethane foaming agent	18,000	1,500

From MIL-HDBK-263 APPENDIX A

(2) Electrostatic charge of human body during working

A storage box of styrofoam carries electrostatic charges as high as several 10,000 V, at which an electrostatic voltmeter fully deflects. Naturally, personnel who handle semiconductor devices charge. **Table 1-33** shows the result of an experiment conducted to monitor the quantity of electrostatic charge built up by workers while walking or working.

Table 1-33. Electrostatic Charge of Workers (MAX. value)

Floor: vinyl tile

Process	Temperature/humidity	Ordinary shoes		Conductive shoes		Remarks
		Wrist strap		Wrist strap		
		Provided	None	Provided	None	
Bonding	25°C 52%	0 V	320 V	—	120 V	Working
Mount	24°C 50%	0 V	–800 V		–520 V	
Appearance check	23°C 53%		220 V		–120 V	Walking
			160 V		30 V	Working

(3) Organizing working environment (example of countermeasures against electrostatic charge)

Here are specific examples of countermeasures against electrostatic charge. By taking these measures, troubles that may occur in each of your processes can be prevented. **Table 1-34** lists examples of countermeasures implemented by the users of NEC's products.

Table 1-34. Example of Countermeasures against Electrostatic Charge by Users

Location	Countermeasures
Worker	• Use wrist straps (it is recommended to install protective resistors of 100 kΩ to 1 MΩ in series). • Use conductive shoes and anti-static clothes. • Eliminate blankets and cushion made of synthetic fiber, and plastic foot rests.
Storage box	• Do not use storage boxes of styrofoam. • Use conductive container. • Use conductive mats. • Ground
Equipment and test instruments	• Ground • Do not use acrylic substance in measuring parts.
Jig	• Keep the friction between jigs and components (devices) as little as possible (contrive jigs such as to minimize the contact area). • Ground
Conveyer	• Ground (contact with conductive materials) • Use conductive belts.
Others	• Use conductive mats (10^6 to 10^{11}Ω). • Install conductive flooring. • Install humidifier. • Ion blow • Eliminate charging material (acrylics, plastic).

1.9 Thermal Resistance of Package

1.9.1 Definition

Thermal resistance is defined by the following.

$\theta_{J-A} = (T_J - T_A)/P$ [˚C/W] ... (1)
$\theta_{J-C} = (T_J - T_C)/P$ [˚C/W] ... (2)

θ_{J-A} : Junction-to-ambient thermal resistance [˚C/W]
θ_{J-C} : Junction-to-case thermal resistance [˚C/W]
T_J : Junction temperature [˚C]
T_A : Ambient temperature [˚C]
T_C : Case temperature [˚C]
P : Power dissipation [W]

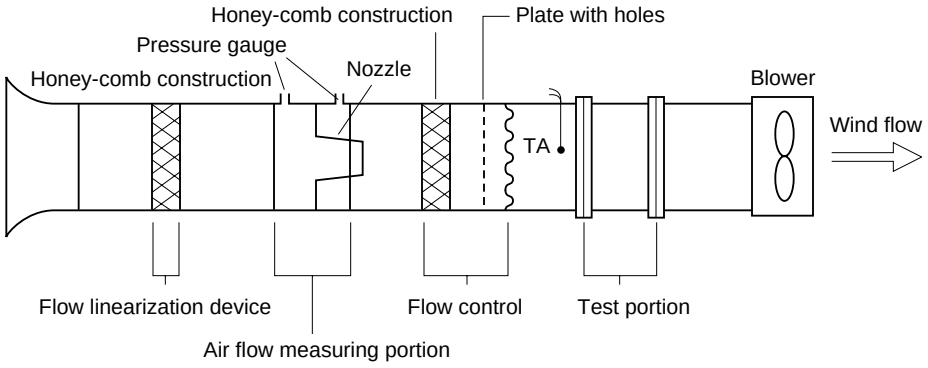
1.9.2 Test method

At NEC, a sample is mounted on a glass-epoxy board (size: 90 × 90 × 1.6 mm) and the thermal resistance is measured as follows.

(1) Tj is measured using the temperature characteristic of the diodes on the chip.
(2) Ta and Tc are measured using a thermocouple. (ex. P = 1[w])
(3) The thermal resistance is calculated from equations (1) and (2).

This measuring method conforms to G38-87 and G43-87. **Figure 1-96** shows a SEMI measuring wind tunnel (sketch).

Figure 1-96. SEMI Wind Tunnel (SEMI G38-87)



1.9.3 Thermal resistance

Table 1-35 shows the thermal resistance of NEC's typical surface mount package.

The thermal resistance varies with the measuring conditions and PWB mounting conditions. Optimization should be made taking into consideration actual use for countermeasures.

Table 1-35. Thermal Resistance Measurements

Package	Package dimension [mm]	Pin No.	Lead frame material	Island area [mm^2]	$\theta_{J\text{-}A}$ [°C/W]			$\theta_{J\text{-}C}$
					0 [m/s]	1 [m/s]	2 [m/s]	[°C/W]
QFP	10 × 10 × 1.0	64	Cu	36	70	56	51	11
	14 × 14 × 1.0	100	Cu	25	75	61	56	12
	14 × 20 × 2.7	64 to 80	Fe-Ni	56	75	63	58	16
	14 × 20 × 2.7	100	Fe-Ni	56	69	57	52	12
	20 × 20 × 1.4	144	Cu	42	57	46	42	5
	28 × 28 × 3.7	120 to 208	Fe-Ni	56	68	58	51	7
	28 × 28 × 3.2	120 to 208	Cu	56	43	35	34	14
	28 × 28 × 3.2 (with heat spreader)	120 to 208	Cu	—	26	19	16	2
TSOP	400 mils 0.97 t	28	Fe-Ni	90	74	56	47	8
QFJ	950 mils 3.4 t	64	Cu	80	42	36	31	4
PBGA	27 × 27 × 1.53	225	—	80	35	29	26	—

PWB material : Glass-epoxy
PWB size : 90 × 90 × 1.6 mm
Wiring density : 15%
T_A measuring point : 6 cm to 7 cm from a sample windward
T_C measuring point : Center of a sample top surface

1.9.4 Calculation examples

Examples of calculations using the thermal resistance are shown below.

[Calculation example 1]

The maximum allowable power dissipation (P_{max}) of a 28 × 28 × 3.2-mm package with a heat spreader is calculated.

Here, the maximum allowable ambient temperature (T_{Amax}) is 85˚C, the joint temperature is 125˚C, and natural air cooling is employed.

The thermal resistance around the joint as derived from **Table 1-35** is 26 ˚C/W.

$$P_{max} = (T_J - T_{Amax})/\theta_{J-A}$$
$$= (125 - 85)/26$$
$$\fallingdotseq 1.5$$

The maximum allowable power dissipation is 1.5 W.

[Calculation example 2]

If the above package is equipped with a 2-W circuit (chip), how many m/s should the velocity of air cooling be?

<1> The thermal resistance of a package that can be equipped with a 2-W circuit is calculated.

$$\theta_{J-A} = (T_J - T_A)/P$$
$$= (125 - 85)/2$$
$$= 20$$

<2> A wind velocity such that θ_{J-A} of the package in **Table 1-35** is 20 ˚C/W or less is calculated.

Air cooling with wind velocity of 1 m/s

1.9.5 Air flow rate

There is a method in which the heat radiation of a package surface is improved with air flow to reduce thermal resistance. **Figure 1-97** shows effect of air flow rate on thermal resistance.

1.9.6 Island area

Figure 1-98 shows effect of island area on thermal resistance. This figure indicates that as the island area increases, its thermal resistance decreases.

Figure 1-97. Airflow rate vs $\theta_{J\text{-}A}$

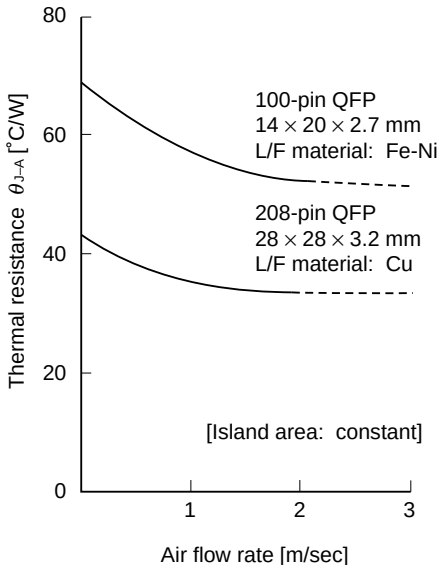
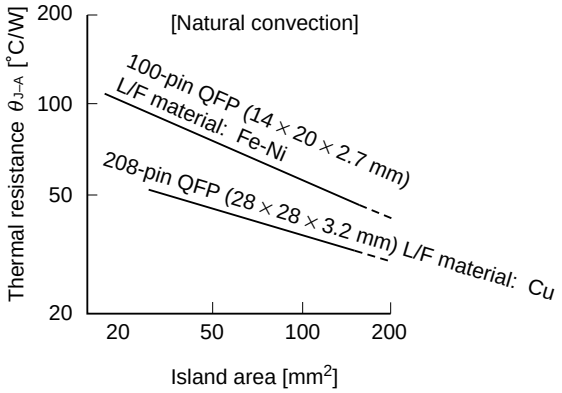


Figure 1-98. Island area vs $\theta_{J\text{-}A}$



1.9.7 Low thermal resistance package

(a) Low thermal resistance QFP

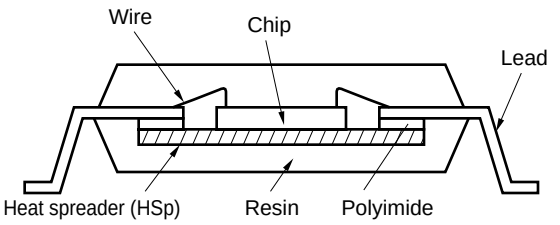
In order to realize a low thermal resistance plastic QFP, the following methods can be employed. One is to replace the lead frame with a high thermal conductivity material (for example, replacing Fe-Ni with Cu). By doing this, the heat from the chip diffuses more easily throughout the package. Another method is to incorporate an internal heat spreader (H/Sp). **Figure 1-99** shows the structure of a conventional package and that of a package incorporating a H/Sp. In the package with H/Sp, the H/Sp, which also serves as a base for chip mounting, is adhered to the package via the inner lead and polyimide film. Since it is made of a Cu board of the same thickness as the lead frame and is incorporated in the package, the external appearance is the same as the conventional type. The reason why the package with H/Sp improves heat radiation is described below.

<1> Since the H/Sp is larger than conventional islands, heat is diffused to the whole package.
<2> Heat tends to transfer from the lead to PWB via the polyimide film.

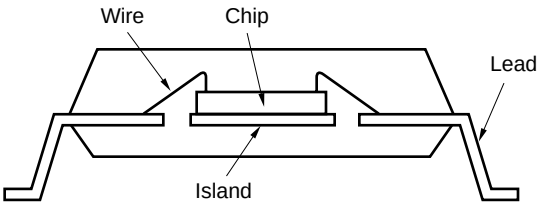
(b) PBGA

As ICs have an increasing number of pins while at the same time miniaturization is demanded, plastic ball grid arrays (PBGA) are gaining attention. PBGAs, compared to QFPs, offer several advantages. One of them is superior heat radiation. **Figure 1-100** shows a sectional drawing of the PBGA, and **Figure 1-101** shows a thermal resistance comparison between the QFP an PBGA. The heat diffusion of the PBGA is good because the heat from the chip escapes from the thermal vias and solder balls set in the PWB under the die pad, to the mounting board.

Figure 1-99. Comparison of QFP Structures



(a) QFP with heat spreader



(b) Conventional QFP

Figure 1-101. Thermal Resistance of QFP and PBGA

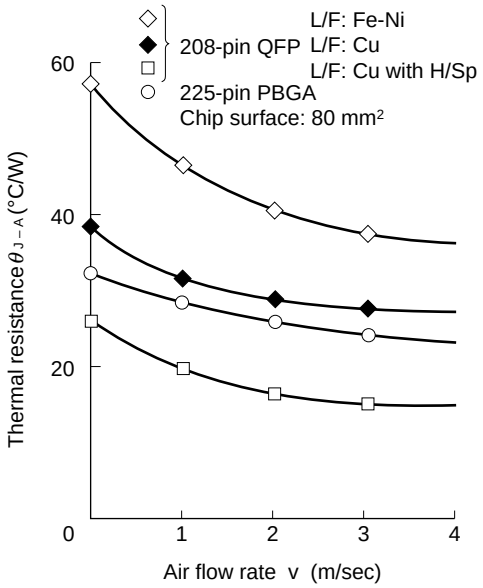
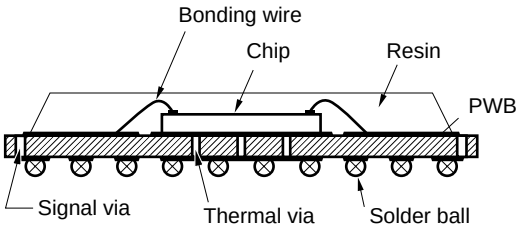


Figure 1-100. Structure of PBGA



1.10 Electrical Characteristics of Package

The electrical characteristics of an IC package consists of the following parameters:

- Pin resistance (R)
- Load capacitance of pin (C)
- Effective inductance of pin (L)

1.10.1 Parameter measurement

NEC determines the electrical characteristic parameters of a package with measurement of actual packages and with simulations.
The following outlines the actual measurement method and simulation.

(1) Measurement method

- **Resistance**
  The DC resistance at a pin is measured using the test circuit shown in **Figure 1-102**. This method complies with the MIL standard.
- **Effective inductance**
  The inductance which occurs through the mutual action of the current flowing the measuring lead and its return current is measured. The inductance is obtained from the voltage drop between sampled edges and the phase difference. The test circuit is shown in **Figure 1-103**. This method complies with the SEMI standard.
- **Load capacitance**
  The capacitance between the test pin and the ground line is measured after all pins except the test pin are connected to the ground line. The capacitance is obtained from the voltage drop between sampled edges and the phase difference. The test circuit is shown in **Figure 1-103**. This method complies with the MIL standard.

Figure 1-102. Test Circuit for Resistance

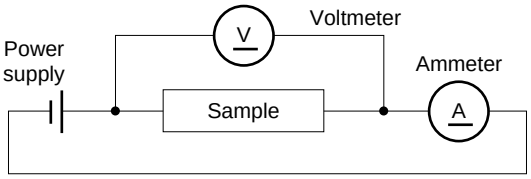
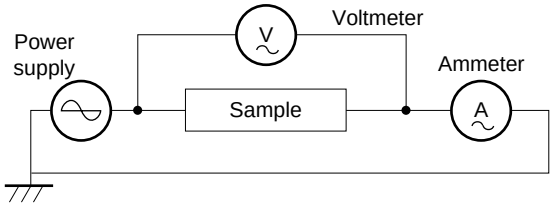


Figure 1-103. Test Circuit for Load Capacitance and Inductance



(2) Simulation

Resistance, capacitance, and inductance can be calculated from the CAD data (such as lead frame and package dimensions) and material characteristics (such as conductivity, magnetivity, inductivity). These values are coherent with actually measured values. Therefore, NEC mainly uses this simulation to obtain electrical characteristics.

1.10.2 Electrical characteristic parameter

The electrical characteristic parameters (R, L, C) of plastic QFPs and plastic BGAs are shown in **Tables 1-36** and **1-37**, respectively.

Since the electrical characteristics parameters are dependent on such conditions as lead frame material, shape, and wiring pattern of the BGA substrate, they may differ even when the packages are the same.

Table 1-36. Electrical Characteristic Parameter of Plastic QFP

(1[MHz])

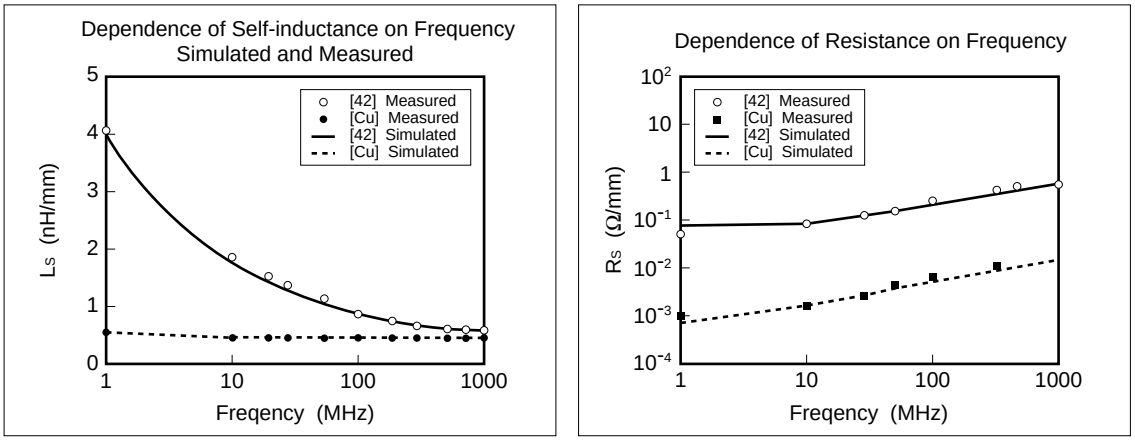
Package	Size (W x D x H)	Pins	Lead frame	R (typ.) [mΩ]	L (typ.) [nH]	C (typ.) [pF]
QFP	14 x 14 x 1.45	100	Fe-Ni	139.2	21.2	0.8
	20 x 20 x 2.7	120	Fe-Ni	143.4	35.5	0.7
	24 x 24 x 2.7	160	Fe-Ni	238.3	63.4	1.4
	28 x 28 x 3.7	160	Fe-Ni	238.0	73.7	1.6
	28 x 28 x 3.2	208	Cu	10.2	9.5	1.3
TQFP	10 x 10 x 1.0	64	Cu	6.4	4.0	0.5
	12 x 12 x 1.05	80	Fe-Ni	161.6	32.1	0.6
	14 x 14 x 1.0	100	Cu	5.9	5.0	0.8
LQFP	12 x 12 x 1.4	64	Cu	4.2	4.9	0.7

Table 1-37. Electrical Characteristic Parameter of Plastic BGA

Number of pins	Pin name	R [mΩ]	L [nH]	C [pF]
225	VDD	99	5.8 max.	—
	GND	108	5.8 max.	—
	Signal	211 to 338	7.9 to 15.1	1.6 to 3.7
256	VDD	105 to 110	6.3 to 8.2	—
	GND	95 to 98	6.1 to 8.0	—
	Signal	120 to 263	5.8 to 14.7	2.1 to 3.3
313	VDD	98 to 103	7.9 to 8.9	—
	GND	93 to 95	5.8 max.	—
	Signal	263 to 383	3.9 to 29.0	2.9 to 3.4

The electrical characteristics parameters are dependent on frequency as well. As the frequency becomes higher, the self-inductance decreases and the resistance increases. **Figure 1-104** shows the frequency characteristics of self-inductance and resistance. As shown also in **1.10.1**, the actually-measured value and the simulated result match.

Figure 1-104. Frequency Characteristics of Self-inductance and Resistance (Simulated and Measured)



CHAPTER 2 THROUGH-HOLE DEVICES (THDs)

2.1 Mounting THDs

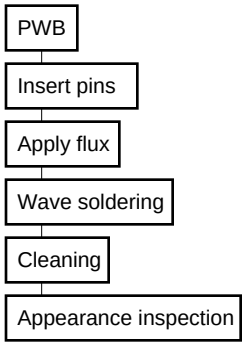
2.1.1 Basic mounting flow

Figure 2-1 shows the basic flow of mounting through-hole devices (THDs).

First, the pins of a THD are inserted into the mating holes on a PWB, and flux is applied to the PWB. Then the PWB is soldered by means of wave soldering (solder flow).

After soldering, the PWB is cleaned to eliminate flux residues deposited during soldering, solder waste (solder balls), and other impurities. Then appearance inspection is conducted.

Figure 2-1. Basic Mounting Flow of THDs



2.1.2 Diameter of hole on PWB

This section describes the relations between positional tolerances and the hole diameter on a PWB, taking a standard DIP as an example.

- Example

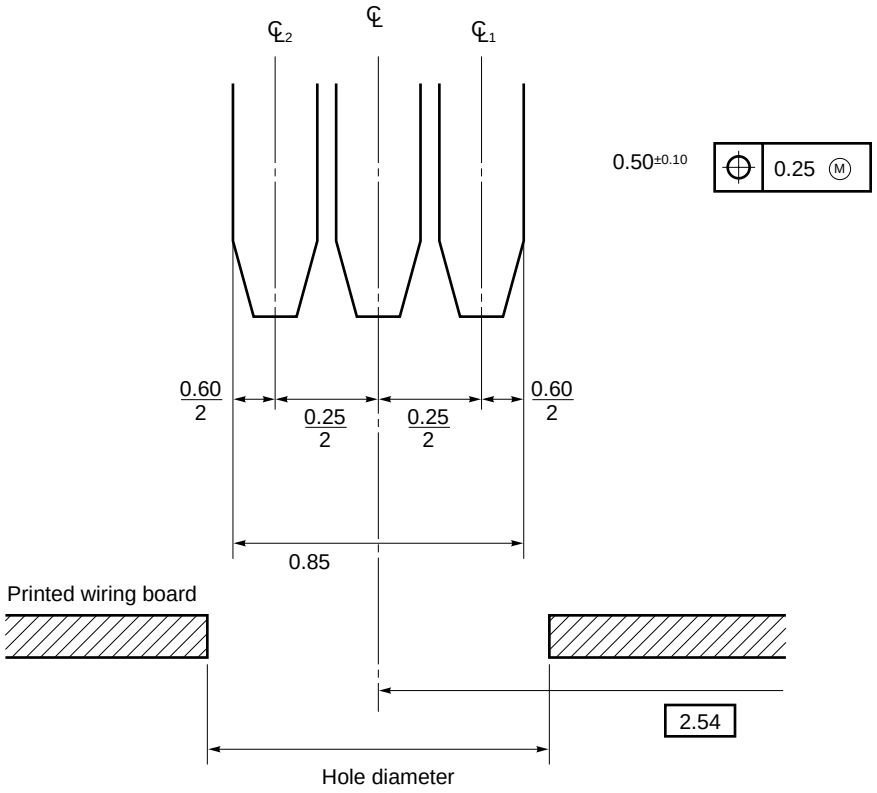
b | ⌖ | 0.25 | Ⓜ | Pin width: This figure indicates that the center of a pin can be shifted up to 0.25 mm from the real center position if the maximum dimension is b. If b is less than the maximum dimension, however, the tolerance can be expanded accordingly.

Figure 2-2 shows the status in which the central position of the pin (℄) is shifted from the real position.

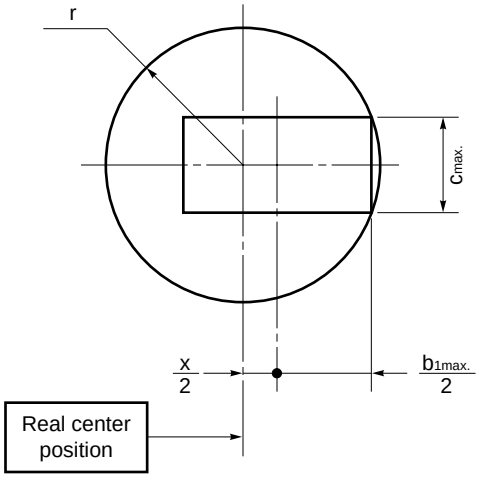
Since the maximum value of pin width $b_{max.}$ = 0.60 mm and tolerance x = 0.25 mm in the case of a standard ZIP, the permissible range in which the pin can exist is as follows:

$$2 \times \left(\frac{x}{2} + \frac{b_{max.}}{2} \right)$$
$$= 2 \times \left(\frac{0.25}{2} + \frac{0.60}{2} \right)$$
$$= 0.85 \text{ mm}$$

Figure 2-2. Relations between Pin Shifted from Center Position and Hole Diameter on PWB



In this case, where the radius of a hole to be drilled on the PWB is r, r can be obtained as follows:



$$r = \sqrt{\left(\frac{x}{2} + \frac{b_{max.}}{2}\right)^2 + \left(\frac{c_{max.}}{2}\right)^2}$$

$$= \sqrt{\left(\frac{0.25}{2} + \frac{0.60}{2}\right)^2 + \left(\frac{0.35}{2}\right)^2}$$

$$= 0.46 \text{ mm}$$

Therefore, the hole diameter is 0.92 mm (MIN.). However, because the tip of the pin is tapered, there is no problem if the pin is inserted into a hole 0.8 mm (MIN.) in diameter.

If the hole diameter is too large, the pin may not be completely soldered.

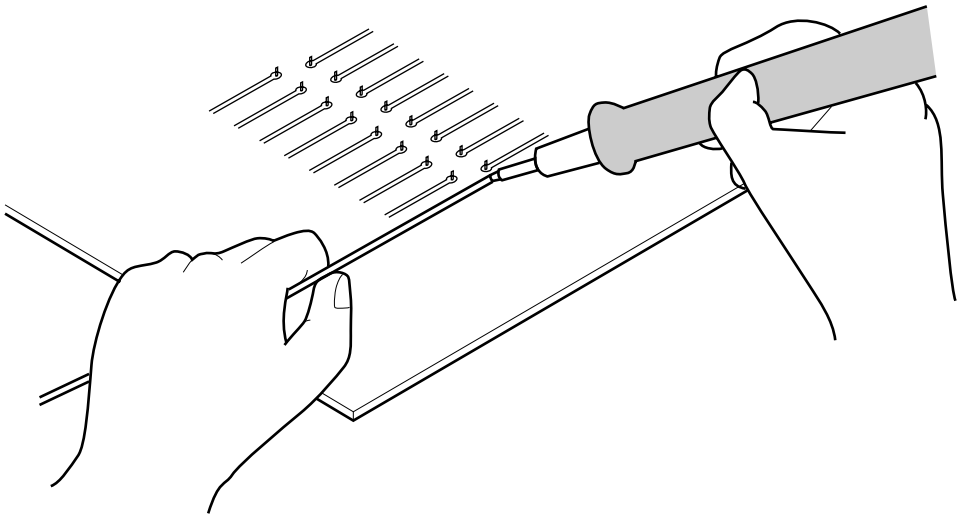
2.1.3 Soldering method

The pins of THD packages are surface-processed (such as solder-plated) so that the THDs can be easily mounted on a PWB. After the pins have been inserted into the mating holes on a PWB, they are usually connected with eutectic solder. The following paragraphs describe the points to be noted in soldering the pins:

(1) With soldering iron

A soldering iron is used for small quantity production. Because the pin pitch of THD is as narrow as 2.54 mm, use of a thin solder of 0.5 mm or less, and an a soldering iron with a thin tip is recommended. The soldering temperature should be kept to 300°C MAX. to reduce the thermal stress imposed on the THD as much as possible. Solder the part of the pin as far away from the body as possible.

Figure 2-3. Soldering with Soldering Iron



Use a soldering iron with low leakage current.

Use of class A soldering irons with an insulation resistance of 10 MΩ MIN. For your reference, here is an excerpt from the statement related to insulation from “Electric Soldering Iron” published by the Japan Industrial Standard (JIS C 9211):

(Reference) JIS C 9211

Insulation: Immediately after temperature measurement, measure the insulation resistance between current-carrying metal part and non-current carrying metal part with insulation resistance meter of 500 V. Confirm that class A has an insulation resistance of 10 MΩ or more and that class B has an insulation resistance of 1 MΩ or more. Apply a voltage of 1000 V at a frequency of 50 or 60 Hz close to sine wave. The sample must endure this voltage for 1 minute.

(2) Dip soldering and wave soldering

These soldering methods are relatively simple. Dip soldering is to dip the copper surface of a PWB (pin side) into the solder bath, while wave soldering is to solder the copper surface of the PWB by jetted solder. Because the PWB is subject to a great thermal stress when it is dipped in the solder bath, these soldering methods must be implemented at 260°C or less and within 10 seconds.

Exercise care in soldering a THD with these methods because if the solder contacts the package body of the THD, the reliability of the device may be degraded.

Confirm that the commercial power supply current is not leaking and ground the soldering bath with a resistor of about 1 MΩ.

Figure 2-4. Dip Soldering

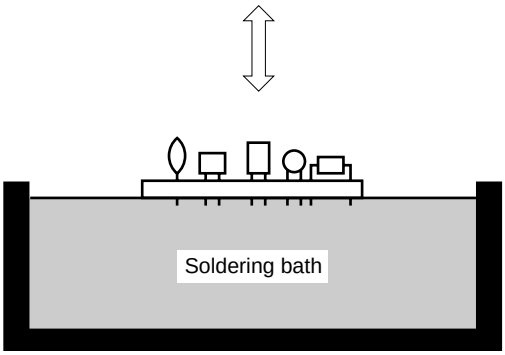
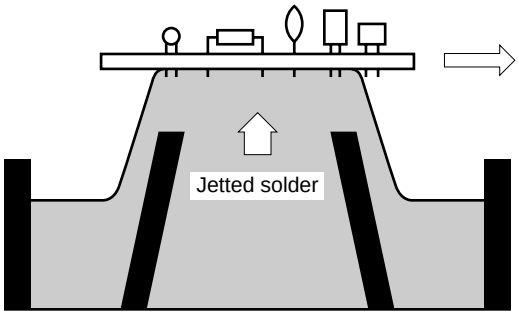


Figure 2-5. Wave Soldering



2.1.4 Notes on mounting

Bear in mind the following points when mounting THDs on a PWB:

(1) Do not allow the bottom surface of THD to contact the PWB.

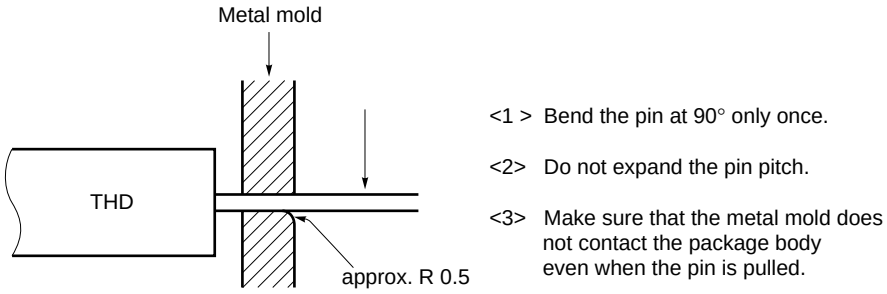
Provide a distance (0.3 mm MIN.) between the PWB and the bottom surface of the THD, so that cleaning flux is easy, that heat generated in THD can be effectively radiated to prevent the temperature of the THD from rising, and that force that may deform the pins of the THD is not applied.

(2) Do not apply excessive force to the pins.

To form the pins of a THD into a desired shape, securely fix the part of the pins close to the bottom surface with pincers or a jig. Especially when a metal mold is used as shown in **Figure 2-6** exercise care that no tensile force is applied to the part of the pins close to the package.

To remove the THD from the PWB, do not apply force to the pins with the tip of a heated soldering iron.

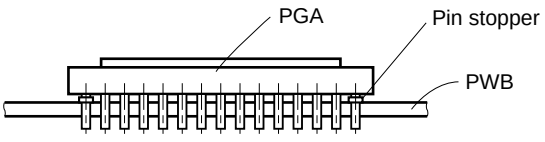
Figure 2-6. Shaping Pin with Metal Mold



(3) Mounting PGA on PWB

Some pins of a PGA are provided with a stopper to provide a distance between the PWB and the bottom surface of the PGA, in order to <1> radiate heat and <2> alleviate mechanical stress imposed on the package. Make sure that these stoppers are effectively used to provide a distance from the PWB (refer to **Figure 2-7**).

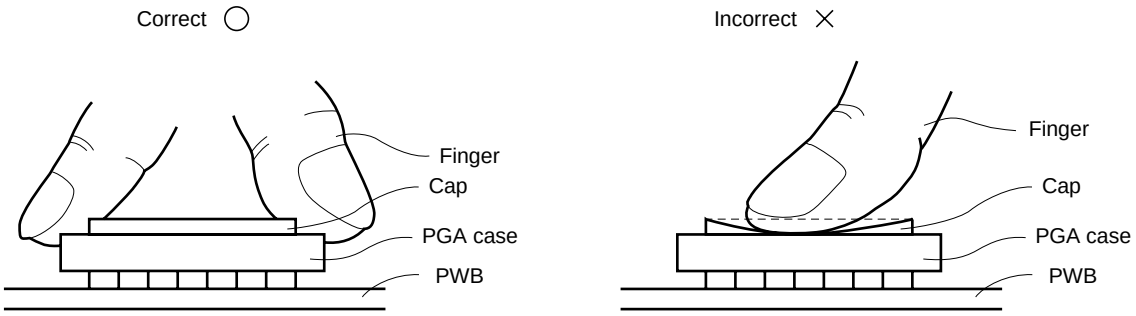
Figure 2-7. Mounting PGA on PWB



Especially in the case of a seam weld type PGA package, if the cap is pressed with your finger when the package is mounted on the PWB*, the cap caves in and the package may be damaged. Mount the package holding the peripheral part of the package with your fingers (refer to **Figure 2-8**).

* The same applies when inserting a socket.

Figure 2-8. Mounting Seam Weld Type PGA on PWB



2.1.5 Type of flux and cleaning

For details on flux cleaning, refer to **CHAPTER 1 SURFACE MOUNT SEMICONDUCTOR DEVICES** (**1.2.7 Types of fluxes and cleaning** and **1.5.6 Evaluation examples related to cleaning and non-cleaning**).

2.2 Recommended Conditions of THDs

2.2.1 Recommended soldering conditions

To solder a THD, partial heating method by which only the pins of the THD are heated is recommended.

For soldering optical semiconductor devices, consult NEC.

(1) Wave soldering

- Peak temperature: 260°C (molten solder temperature)
- Soldering time: 10 seconds MAX.

Make sure that flow solder does not come in contact with the package when the THD is soldered.

(2) By soldering iron

- Peak temperature: 300°C (pin temperature)
- Time: 3 seconds MAX. (per 1 pin)

2.2.2 Recommended cleaning conditions

For the recommended flux cleaning conditions, refer to **CHAPTER 1 SURFACE MOUNT SEMICONDUCTOR DEVICES** (**1.4.2 Recommended conditions of flux cleaning and non-cleaning flux**).

When performing ultrasonic cleaning, confirm in advance that no problem occurs because of resonance.

2.3 Packing of THD

2.3.1 Packing style

THDs are housed in various packages such as DIP, SIP, ZIP, and QUIP, and are available in various packing styles including tapes, magazines and trays.

So that you can understand the package dimensions and packing styles of NEC's THDs and SMDs, the following information document is readily available:

Semiconductor Device Package Manual (document number: C10943X)

There are some cautions that you must bear in mind when handling IC packages. Refer to **CHAPTER 1 SURFACE MOUNT SEMICONDUCTOR DEVICES** (**1.7.1 (2) Notes on handling (a)** through **(C)**).

APPENDIX A REFERENCE

A.1 IC Package Terms

The terms used in the IC package are described below.
These terms were created with reference to EIAJ and JEDEC terms.

Terms		Description
BGA	Ball Grid Array	Package whose connecting soldering balls are arranged in grid at its base.
CERDIP (DIP-G)	Ceramic Dual In-line (DIP-Glass)	Hollow package made airtight by sealing two molten ceramic plates with melted glass.
COB	Chip On Board	Insulated board made of ceramic, etc. on which conductive patterns formed, chips are mounted and bonded, and sealed with resin.
DIP	Dual In-Line Package	e = 100 mils (2.54 mm) 2-terminal row package whose pins forming dual-in line from the package body are drawn out, so that the package can be inserted in the PWB holes and mounted.
FBGA	Fine-pitch BGA	BGA with ball pitch of less than 0.8 mm.
LQFP	Low-profile QFP	QFP with a thickness of 1.4 mm and mounting height of less than 1.7 mm.
PGA	Pin Grid Array	Square package whose external pins facing the package mounting surface from the package body base are arranged at intervals of 100 mil (2.54 mm) in grid, so that the package can be inserted in the PWB and mounted.
Plastic PGA	Plastic PGA	PGA package made of plastic.
QFJ (PLCC)	Quad Flat J-Leaded Package (Plastic Leaded Chip Carrier)	Package whose pins are drawn out in four directions from the package body and whose pins at the external contact part face inwards to form a J shape, so that the package can be mounted on the PWB surface.
QFN (LCC)	Quad Flat Non-Leaded Package (Leadless Chip Carrier)	Non-leaded package with solder mount sections in four directions of the exterior circumference of the package base, so that the package can be mounted on the PWB surface.
QFP	Quad Flat Package	Package whose pins are drawn out in four directions from the package body and whose pins at the external contact part face outwards to form a L shape, so that the package can be mounted on the PWB surface.

Terms		Description
QTP	Quad Tape Carrier Package	Package where copper film patterns are formed on the insulated tape face with sprocket hall and pins project out from four directions parallel to the mounting surface at the exterior.
QUIP	Quad In-line Package	Minimum pin interval [e] = 50 mils (1.27 mm) 4-terminal row package whose pins forming dual-in line from the package body are drawn out, so that the package can be inserted in the PWB and mounted.
SDIP	Shrink DIP	[e] = 70 mils (1.778 mm) DIP
SOP	Small Out-line Package	[e] = 50 mils (1.27 mm) 2-terminal row package whose pins forming dual-in line the longer side of the package body are drawn out, and whose contact part pins face outwards and are flat at the exterior of the package, so that the package can be mounted on the PWB surface.
SSOP	Shrink SOP	[e] ≤ 1.0 mm SOP
SIM	Single In-line Module	[e] = 100 mils (2.54 mm) single in-line whose electrodes or pins are drawn out in one direction of the module, so that the package can be inserted and mounted on the PWB.
SIP	Single In-line Package	1-terminal row package whose pins are drawn out in one direction from the package body, so that the package can be inserted in the PWB holes and mounted.
SOI	Small Out-line I-lead Package	Package whose pins are drawn out in two directions from the package body and whose pins at the external contact part face downwards to form a I shape, so that the package can be mounted on the PWB surface.
SOJ	Small Out-line J-lead Package	Package whose pins are drawn out in two directions from the package body and whose pins at the external contact part face inwards to form a J shape, so that the package can be mounted on the PWB surface.
SPGA	Shrink PGA	[e] ≤ 1.27 mm PGA package whose pins form an I shape so that the package can be mounted on the surface.
SVP	Surface Vertical Package	Package whose pins are drawn out in one direction from the package body and whose pins at the external contact part form a L shape.
TCP (TAB)	Tape Carrier Package (Tape Automated Bonding)	Tape in which the chip with the bump is connected to inner leads of the insulated film on which a copper film pattern is formed.
TQFP	Thin QFP	QFP with mounting height of less than 1.27 mm.
TSOP (I)	Thin SOP (Type I)	SOP whose mounting height is less than 1.20 mm and whose pin interval is less than 0.8 mm.
TSOP (II)	Thin SOP (Type II)	SOP whose mounting height is less than 1.20 mm, pin interval is less than 1.27 mm.
TSSOP	Thin SSOP	SSOP with mounting height of less than 1.20 mm.

Terms		Description
V-DIP	Vertical Dual In-line Package	Vertical dual in-line package whose pins project out in one direction are drawn out, so that the package can be inserted in the holes of the PWB and mounted.
ZIP	Zig-zag In-line Package	Package whose pin row interval is made 100 mils (2.54 mm) by drawing out external pins 50 mils (1.27 mm) towards the mounting surface of the package from the base side, and to enable pin insertion, external pins are bent alternately inside the package.

As the following external dimensions rules were established according to EIAJ, use it as a reference.
ED-7401-2 semiconductor package names and codes (integrated circuit) (Revised in June 1994)

A.2 EIAJ Specifications

The EIAJ specifications were established by the Technical Standardization Committee on Semiconductor Device Package: EE-13 composed of semiconductor manufacturers, package manufacturers, socket manufacturers, etc. The specifications related to the main packages specified by this committee are as follows.

○ Integrated Circuit External Dimensions Rules (Including those under discussion currently)

ED-7401A	Semiconductor device standard external drawings preparation standards (IC) (December 1995)
ED-7401-1	Semiconductor device external demensions rules preparation manual (IC) (June 1994)
ED-7401-2	Semiconductor device names and codes (IC) (Revised in June 1994)
ED-7401-4	Method of measuring semiconductor device package dimensions (IC) (May 1995)
ED-7402-1	Small out-line package SOP (February 10, 1989)
ED-7402-2A	Shrink small out-line package SSOP (Revised in November 1993)
ED-7403-1	Plastic dual in-line package DIP-P (April 28, 1988)
ED-7405	Zig-zag in-line package ZIP (October 1991)
ED-7405-1	Shrink zig-zag in-line package SZIP (March 1990)
ED-7406A	Small out-line J-lead package SOJ (May 26, 1988)
ED-7407	Quad flat J-lead package QFJ (June 23, 1988)
ED-7408A	Pin grid array package PGA (Revised in February 1994)
ED-7409	Quad flat I-lead package QFI (June 23, 1988)
ED-7410	Small out-line I-lead package SOI (June 23, 1988)
ED-7412	Quad flat leadless package QFN (November 25, 1988)
ED-7413	Single in-line package SIP (January 26, 1989)
ED-7414	Guard ring quad flat package GQFP (November 1989)
ED-7415	Small out-line package with heat sink HSOP (November 1989)
ED-7417	Bumpered quad flat package BQFP (February 1990)
ED-7418	Glass shield quad flat package QFP-G (July 1990)
ED-7419	Glass shield dual in-line package DIP-G (September 1990)
ED-7421	Ceramic dual in-line package DIP-C (October 1991)
ED-7422	Glass shield quad flat J-lead package QFJ-G (October 1992)
ED-7423	Ceramic quad flat J-lead package QFJ-C (February 1993)
ED-7424	Vertical surface mount package SVP (December 1993)
ED-7431A	Quad tape carrier package QTP (April 1993)
ED-7432	Dual tape carrier package (Type I) DTP (I) (December 1993)
ED-7433	Dual tape carrier package (Type II) DTP (II) (December 1993)
EDR-7311	Design guideline of integrated circuits (QFP) (April 1996)
EDR-7312	Design guideline of integrated circuits (TSOP I) (April 1996)
EDR-7313	Design guideline of integrated circuits (TSOP II) (April 1996)

○ These rules and specifications are available at EIAJ.

EIAJ Standardization Center
No. 8 Toyo Kaiji Bldg., 6F 1-5-13 Nishi Shimbashi, Minato-ku, Tokyo 105
TEL: 03-5251-0562

A.3 Daisy Chain[Note] Wiring Diagrams for BGA Packages

NEC provides users with mechanical samples of BGA which are prewired in daisy chain. These samples allow users to do a conductivity test after a BGA fien pitch BGA is mounted.

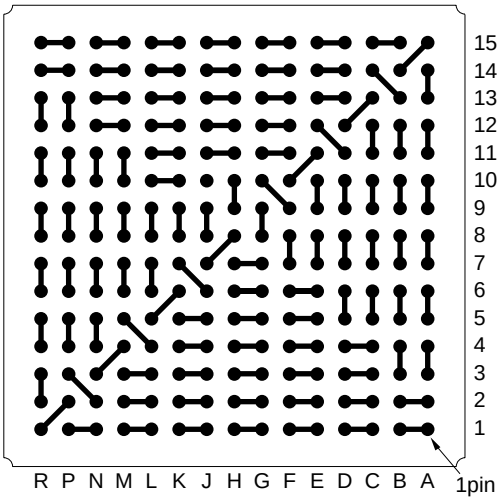
The following pages show the daisy chain wiring diagrams of plastic BGAs, tape BGAs, and fine-pitch BGA. All diagrams show the image seen from the ball side (from solder bumps).

Note Daisy chain is a type of connection in which each component is connected to its adjacent ones to form a line.

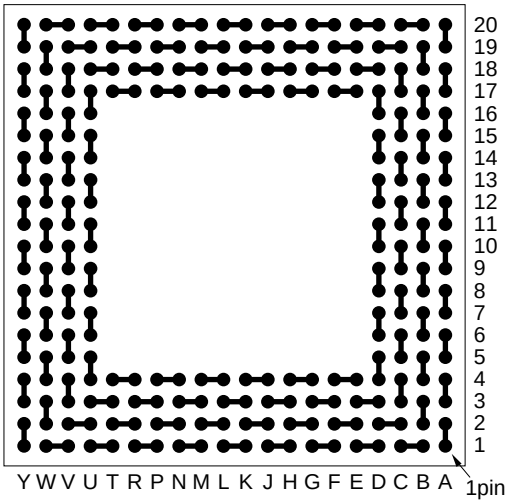
(1) Plastic BGA daisy-chain wiring diagrams

(a) Cavity-up type

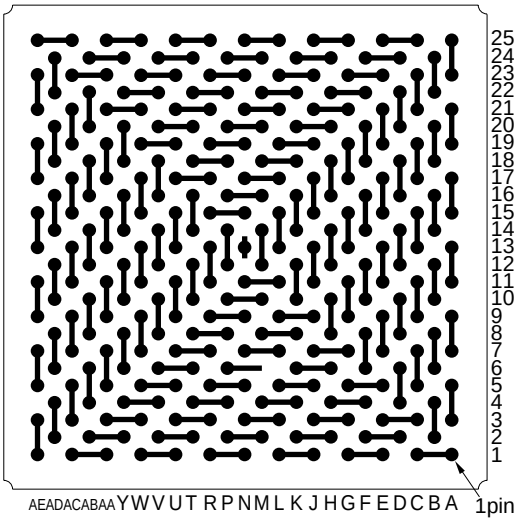
225 pins (27 x 27)



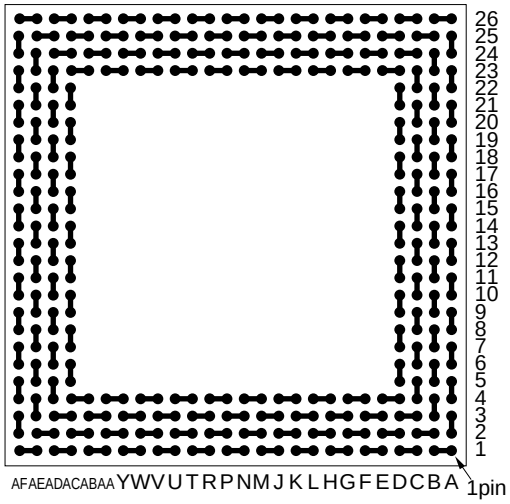
256 pins (27 x 27)



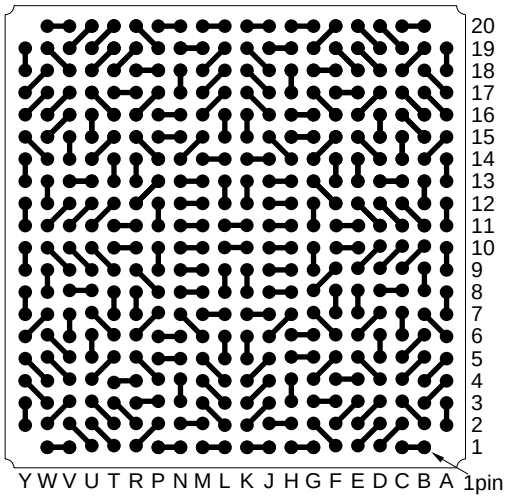
313 pins (35 x 35)



352 pins (35 x 35)

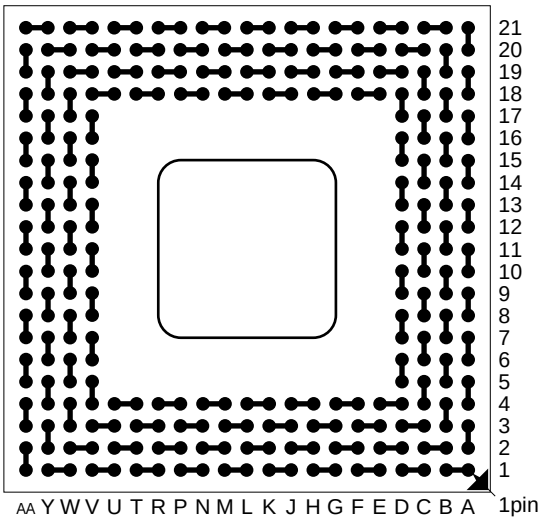


396 pins (35 x 35)

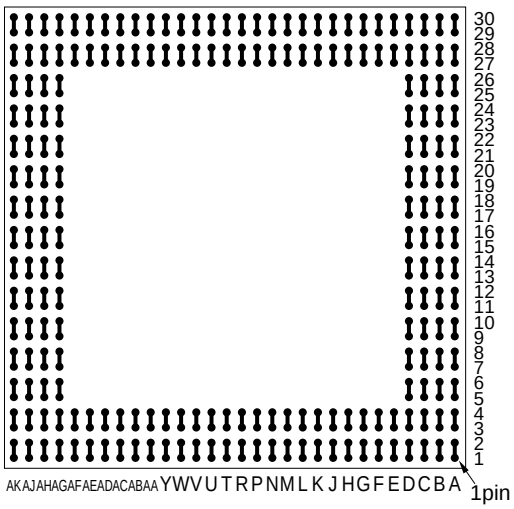


(b) Cavity-down type

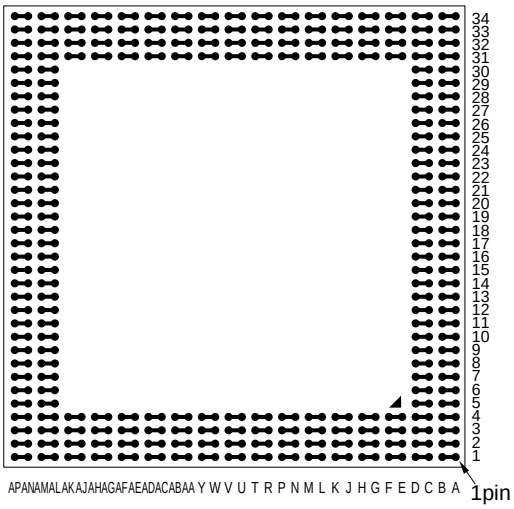
272 pins (29 x 29)



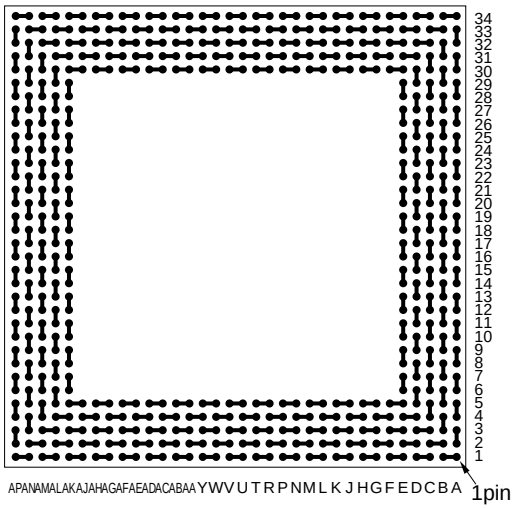
416 pins (40 x 40)



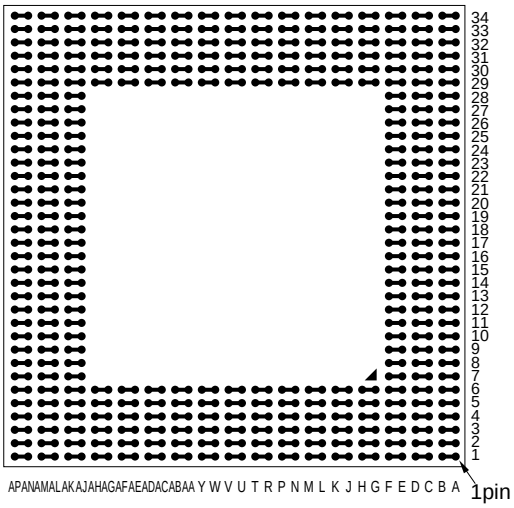
480 pins (45 x 45)



580 pins (45 x 45)

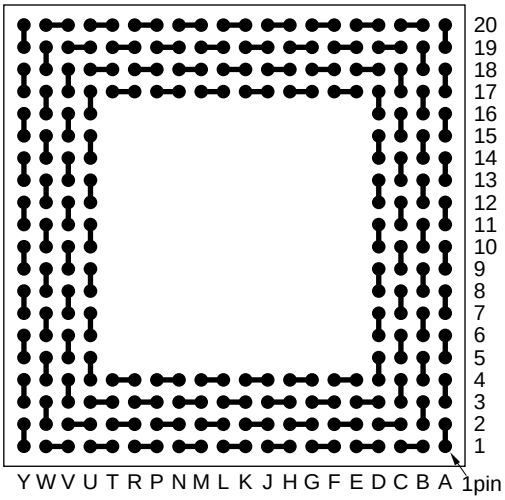


672 pins (45 x 45)

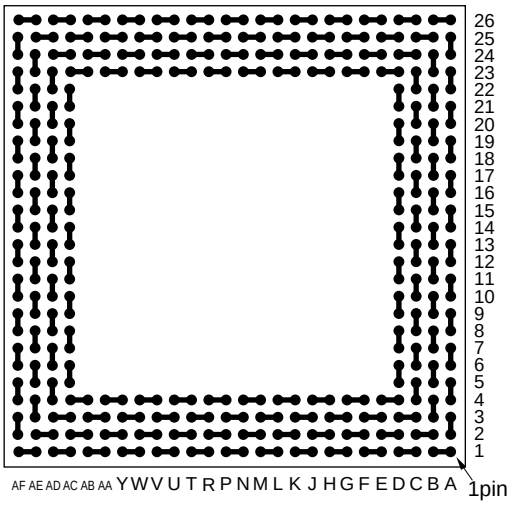


(2) Tape BGA daisy-chain wiring diagrams

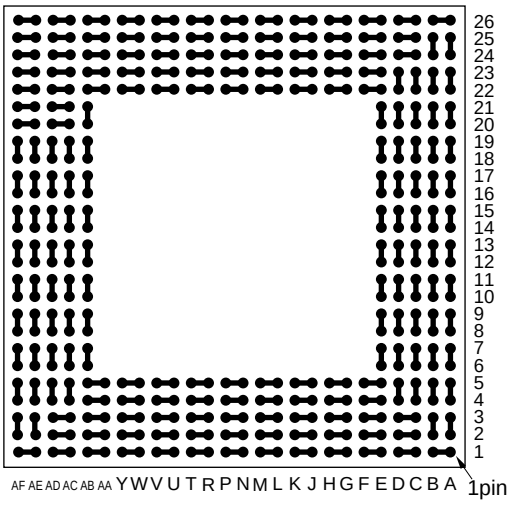
256 pins (27 x 27)



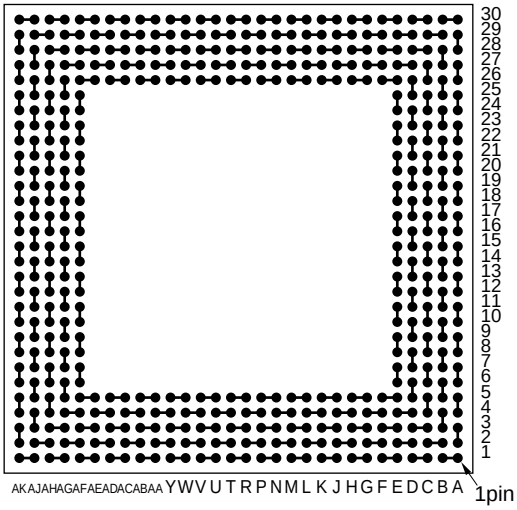
352 pins (35 x 35)



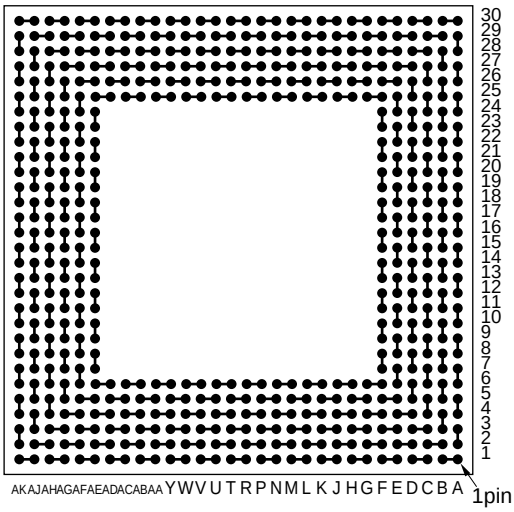
420 pins (35 x 35)



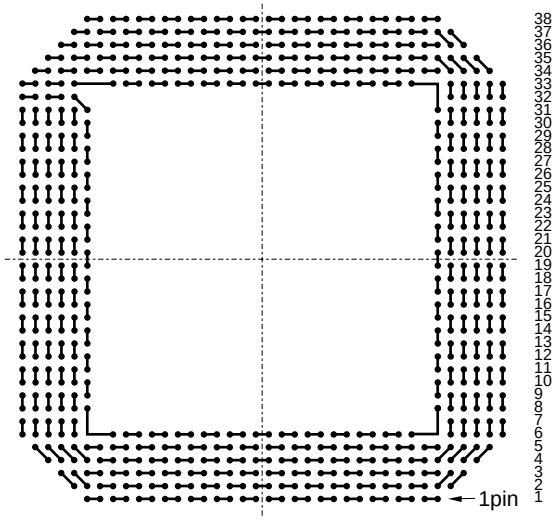
500 pins (40 x 40)



576 pins (40 x 40)

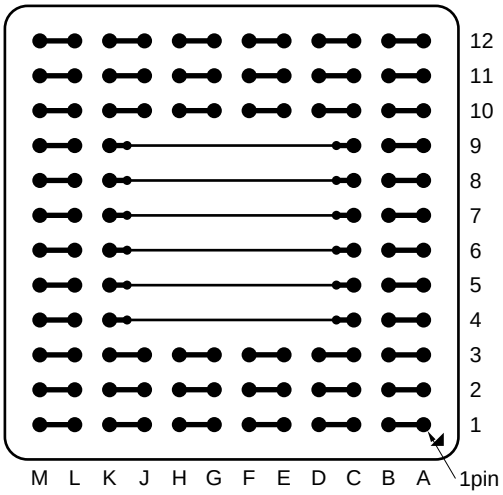


696 pins (40 x 40)

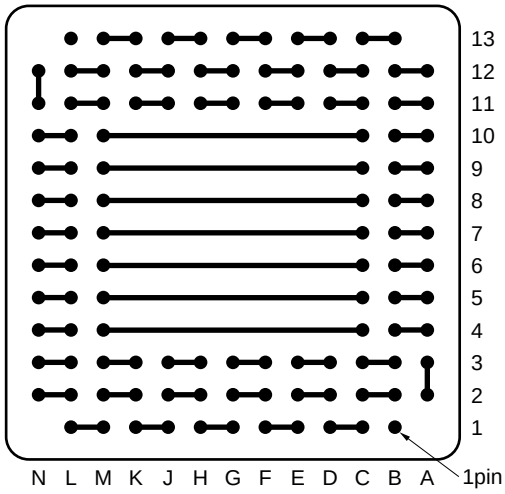


(3) Fine-pitch BGA daisy-chain wiring diagrams

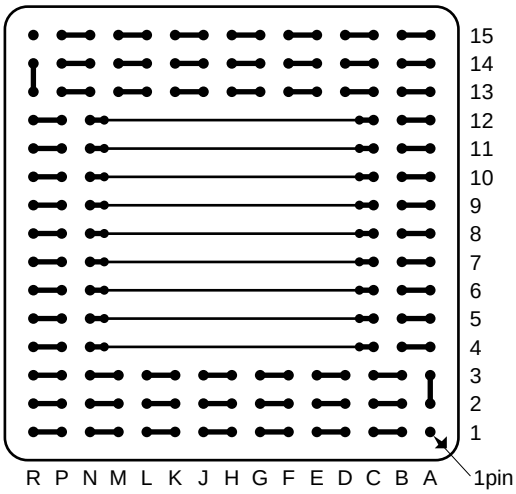
108 pins (11 x 11)



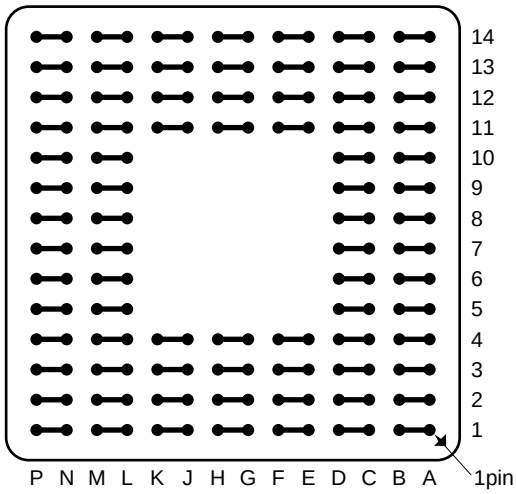
116 pins (12 x 12)



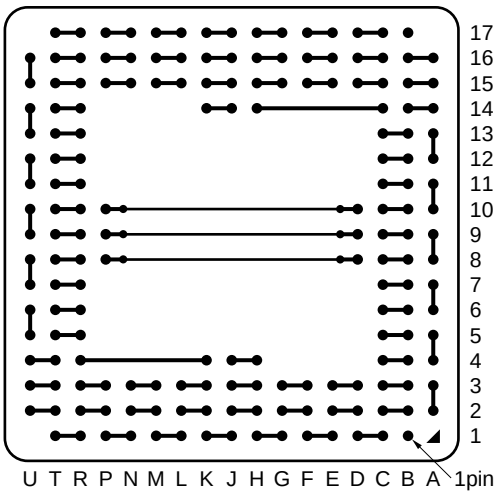
144 pins (13 x 13)



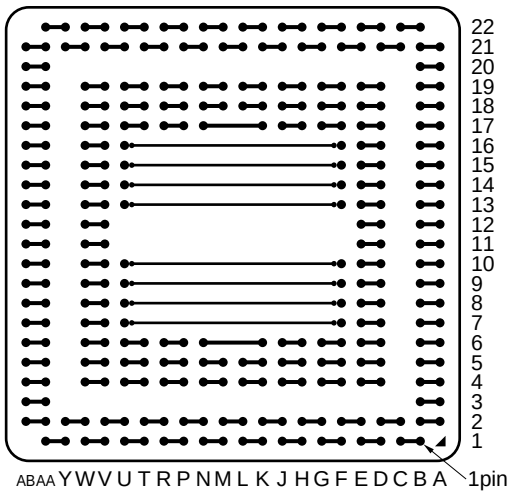
160 pins (13 x 13)



176 pins (15 x 15)



304 pins (19 x 19)



A.4 Example of Designing PWB to Mount BGA

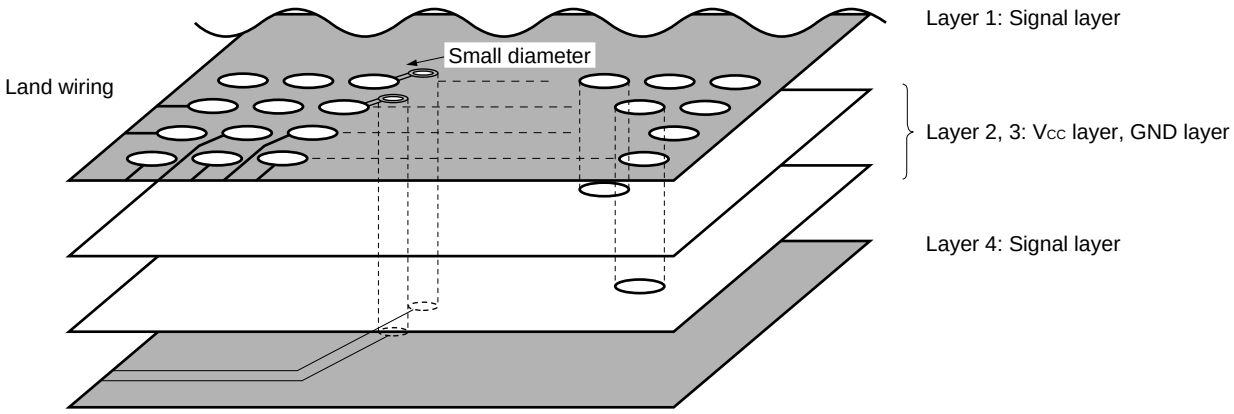
○ Example of designing PWB to mount BGA

Package type	Pin count	Pitch (mm)	Package size (mm)	Ball placement	Line & space (μm)	No. of layer	Pad diameter (mm)
P-BGA	225	1.5	27 x 27	Full matrix	100/150	6	0.6
	256	1.27	27 x 27	4 low	130/180	4	0.6
	313	1.27	35 x 35	Stagger	100/150	4	0.6
	352	1.27	35 x 35	4 low	130/180	4	0.6
	420	1.27	35 x 35	5 low	100/150	4	0.6
T-BGA	256	1.27	27 x 27	4 low	130/180	4	0.6
	352	1.27	35 x 35	4 low	130/180	4	0.6
	420	1.27	35 x 35	5 low	100/150	4	0.6
	500	1.27	40 x 40	5 low	100/150	4	0.6
	576	1.27	40 x 40	6 low	100/150	4	0.6
	696	1	40 x 40	6 low	100/150	6	0.5
C/DPBGA	416	1.27	40 x 40	4 low	130/180	4	0.6
	480	1.27	45 x 45	4 low	130/180	4	0.6
	580	1.27	45 x 45	5 low	100/150	4	0.6
	672	1.27	45 x 45	6 low	100/150	4	0.6

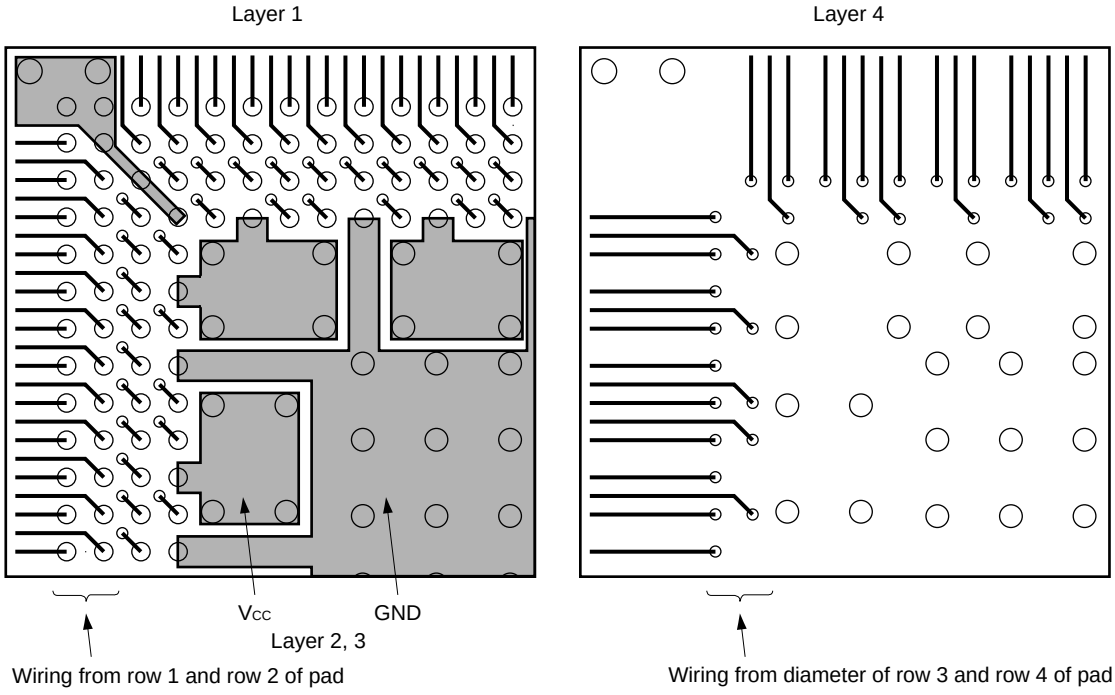
- Pad note: 1/2 pin pitch
- Pad specification: over-resist (no resist stub)

○ PWB cross-section

Example of material: FR-4/board thickness: 1.6 mm



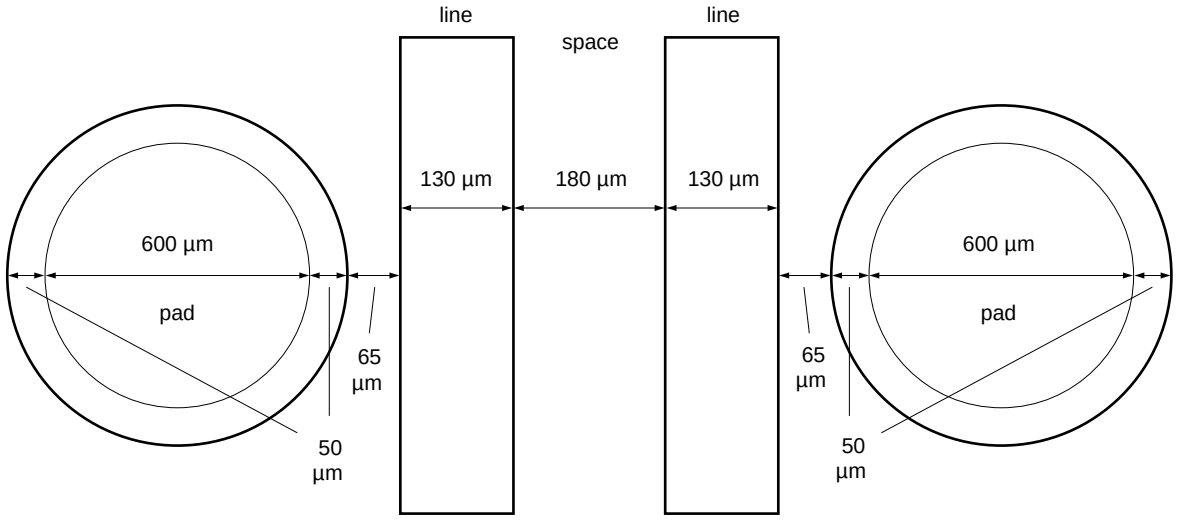
○ **Example of 352-pin PWB layout**



○ **PWB specification of 352-pin P-BGA**

- Material : FR-4
- Board thickness : 1.6 mm
- Pad diameter : ϕ0.6 mm
- VIA diameter (inside diameter) : ϕ0.5 mm
- L/S : 130 μm/180 μm
- Wiring thickness : 35 μm
- Pin pitch : 3-pin specification

Example 352-pin line & space on PWB



- 65 μm is the gap between 130 μm wiring and overresist.
- Pad specification: Pad diameter: ϕ0.6 mm, resist diameter: ϕ0.7 mm

A.5 Reference Example of Reworking Conditions of BGA Package

○ Reference example of reworking setting conditions of BGA package (Reworking equipment: HG7900 made by M&M PRODUCTS Inc.)

Package specifications			UP heater	Bottom heater	AIR flow rate	Heat time	Power condition	PWB spec.
Package type	Pins	Dimensions	(˚C)	(˚C)	(L/min.)	(sec)		
PBGA	Ompac 225 pins	27 x 27	320	250	25	120 to 150	High	FR-4
	Ompac 256 pins	27 x 27						4 layer
	C/D 416 pins	40 x 40	400	300	30	150 to 180		1.6 mm
	C/D 480 pins	45 x 45						(thickness)
	C/D 580 pins	45 x 45						
	C/D 672 pins	45 x 45						
TBGA	256 pins	27 x 27	360	200	30	150 to 180		
	352 pins	35 x 35						
	420 pins	35 x 35						
	500 pins	40 x 40						
	576 pins	40 x 40						
	696 pins	40 x 40						
FBGA	116 pins	12 x 12	400	200	25	30 to 70	Low	FR-4
								4 layer
								0.8 mm
								(thickness)

A.6 Plastic-BGA Sockets

The following table lists the manufacturers and their part numbers of plastic-BGA socket.

Plastic BGA Sockets and Manufacturers

Pins	Manufacturer	Part number
225	Enplas	BGA-225-1.5-01A
	Sumitomo 3M	2-0225-08172-000-019-002
256	Enplas	BGA-256(441)-1.27-1-1.5-01
	Sumitomo 3M	2-0256-08313-050-019-002
313	Enplas	BGA-313-(841)-1.27-01
	Sumitomo 3M	2-0313-08202-110-019-002
352	Enplas	BGA-352(841)-1.27-01
	Sumitomo 3M	2-0352-08334-000-019-002
292	Enplas	BGA-292(441)-1.27-02
388	Enplas	BGA-388(841)-1.27-01
	Sumitomo 3M	2-0338-08392-000-019-002
416	Sumitomo 3M	2-0416-08516-050-019-002
480	Sumitomo 3M	2480-1383-NP-1902
580	Sumitomo 3M	2-0580-08562-000-019-002
672	Sumitomo 3M	2-0672-08407-050-019-002

For details on the specifications and dimensions of these products, call:

Enplas Corp.: 048-643-7676 (Japan)

Sumitomo 3M Corp.: 0423-62-1464 (Japan)

A.7 Materials and Devices Manufacturers

Item		Manufacturer	Contact
Materials	Adhesive	Hiroki	03-3529-5311
		Somaru	03-3542-2175
		Three Bond	0426-61-1333
		Matsushita Denki Sangyou Seiki Jigyoubu	0552-75-6222
	Solder paste	Senju Kinzoku Kogyou	03-3888-5151
		Manufacturer: Nippon Alphametals	0463-32-8130
		Dealer: Tanaka Kikinzoku	03-3668-2124
		Nihon Handa	03-3624-5771
		Harima Kasei	03-3555-3033
		Tamura Seisakujo Co., Ltd. Sales Dept.	03-3978-2111
		Nippon Superia-sha	06-380-1121
	VPS agent	Manufacturer: 3M (USA)	
		Dealer: Sumitomo 3M Tokyo Branch	03-3709-8541
		Manufacturer: ISC Chemical	
		Dealer: Sumitomo 3M Tokyo Branch	03-3709-8541
		Manufacturer: Montefiuos. S. P. A. (Italy)	
		Dealer: Nippon Montezison	03-3797-3973
		Tokuyama Soda	03-3597-5027
	Cleanser	Manufacturer: Nippon Alphametals	0463-32-8130
		Dealer: Tanaka Kikinzoku	03-3668-2124
		Henkeru Hakusui	06-231-9281
		Kao Kagakuhin Jigyoubu	03-3660-7663
		Arakawa Kagaku Kogyou	06-209-8634
Devices	Printer	Senju Kinzoku Kogyou	03-3888-5151
		Manufacturer: Fujioka Seisakujo	
		Dealer: Hiroki	03-3529-5311
		Murakami Screen	03-3625-8125
		Matsushita Denki Sangyou Seiki Jigyoubu	0552-75-6222
		Mitani Densi Kogyou	0427-36-2288
	Dispenser	Iwashita Engineering	03-3458-3401
		Musashi Engineering	0422-33-8111
	Mounter	Fuji Kikai Seizou Tokyo Branch	0566-81-2111
		TDK Co., Ltd.	03-3278-5106
		Matsushita Denki Sangyou Seiki Jigyoubu	0552-75-6222
		Nippon Dynaba-do	03-3661-8861
		M&M PRODUCTS INC.	03-3756-9786
	Paper reflow	Tekunoalpha	03-3280-6466

Item		Manufacturer	Contact
Devices	Laser reflow	NEC Corporation FA Systems Sales Dept.	03-3798-6354
	Infrared, hot air reflow	Senju Kinzoku Kogyou Yokota Kikai Hiroki Ja-do Eitec Tekutoron	03-3888-5151 0426-25-5511 03-3529-5311 03-3942-5861 0426-26-4888
	Hot-air (For repair)	Manufacturer: M&M PRODUCTS INC. Dealer: Houshou	03-3756-9986 03-3274-2431
	Cleanser	Asuka Seiki Sangyou	03-5684-8611
	Ultrasonic crack inspector	Hitachi Kenki Canon Hanbai Toshiba Co., Ltd. Sales Dept. 2	03-3245-6321 03-3740-3334 03-3457-4246
	Appearance inspection unit	NEC Corporation FA Systems Sales Dept.	03-3798-6195

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