SD68C32
SD68C32L

High Performance
32K x 8 CMOS SRAM

Features

- **Single +5V (±10%) VCC for 12/15/20ns**
- **Single +5V (±5%) VCC for -8/10ns**
- **High Speed**
  - **Equal access and cycle time**
  - **8/10/12/15/20 ns access time**
- **Low-power consumption**
  - **Active: 100mA (10 ns cycle)**
  - **Stand-by: 5mA (CMOS input/output)**
    20mA (TTL input/output)
- **Easy memory expansion with $\overline{CE1}$, and $\overline{OE}$ inputs**
- **2.0V data retention mode**
- **TTL compatible, Tri-state input/output**
- **Automatic power-down when deselected**

Functional Description

SD68C32 is a high-performance CMOS Static RAM organized as 31,768 words by 8 bits. Easy memory expansion is provided by an active LOW $\overline{CE1}$, and active LOW $\overline{OE}$, and Tri-state I/O's.

Writing to the device is accomplished by taking Chip Enable 1 ($\overline{CE1}$) with Write Enable ($\overline{WE}$) LOW.

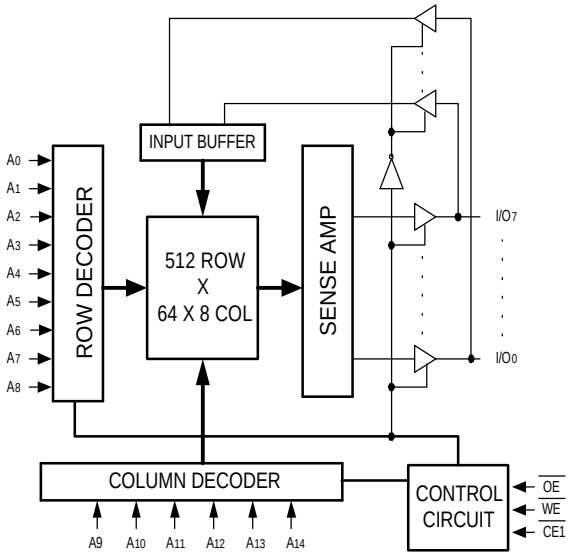
Reading from the device is performed by taking Chip Enable 1 ($\overline{CE1}$) with Output Enable ($\overline{OE}$) LOW while Write Enable ($\overline{WE}$) is HIGH.

I/O pins are placed in a high-impedance state when device is deselected; outputs are disabled during a write cycle.

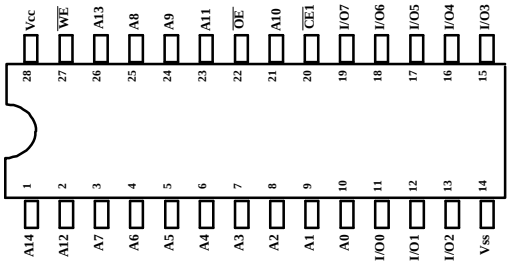
The SD68C32L is functionally the same as the SD68C32. The only difference is the SD68C32L comes with a 2V data retention feature.

SD68C32 is available in a 28-pin, 300 mil Plastic SOJ, and 8x20/ 8x13.4 mm TSOP1 packages.

Logic Block Diagram



28-Pin SOJ



28-Pin TSOP1

Rev. 11/99

20410 TOWN CENTER LANE, STE 270 • CUPERTINO, CA 95014 • TEL (408) 255-1262 • FAX (408) 255-1359

Absolute Maximum Ratings *

Parameter	Symbol	Minimum	Maximum	Unit
Voltage on Any Pin Relative to Gnd	Vt	-0.5	+7.0	V
Power Dissipation	PT	–	1.0	W
Storage Temperature (Plastic)	Tstg	-55	+150	^{0}C
Temperature Under Bias	Tbias	-10	+85	^{0}C

*** Note:** Stresses greater than those listed above Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth Table

$\overline{CE1}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High-Z	Standby
L	H	L	Data Out	Active, Read
L	H	H	High-Z	Active, Output Disable
L	L	X	Data In	Active, Write

*** Key:** X = Don't Care, L = Low, H = High

Recommended Operating Conditions ($T_A = 0^0C$ to $+70^0C$)

Parameter*	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	Gnd	0.0	0.0	0.0	V
Input Voltage	V_{IH}	2.2	-	V_{CC} + 0.5	V
	V_{IL}	-0.5*	-	0.8	V

***** V_{IL} min = -3.0V for pulse width less than $t_{RC}/2$.

DC Operating Characteristics (V_{cc} = 5V±5%/10%, Gnd = 0V, T_A = 0^0C to +70^0C)

Parameter	Sym	Test Conditions	-8		-10		-12		-15		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	$\|I_{LI}\|$	V_{cc} = Max, V_{in} = Gnd to V_{cc}	-	5	-	5	-	5	-	5	µA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CE1}$ = V_{IH} V_{cc}= Max, V_{OUT} = Gnd to V_{cc}	-	5	-	5	-	5	-	5	µA
Operating Power Supply Current	I_{CC}	$\overline{CE1}$ = V_{IL} I_{OUT} = 0, f = f_{max}	-	120	-	100	-	95	-	90	mA
		L	***-***	***100***	***-***	***80***	***-***	***75***	***-***	***70***	
Standby Power Supply Current (TTL Level)	I_{SB}	$\overline{CE1}$ = V_{IH} f = f_{max}	-	20	-	20	-	20	-	20	mA
Standby Power Supply Current (CMOS Level)	I_{SB1}	$\overline{CE1}$ ≥ V_{cc} - 0.2V , f=0 V_{IN} ≤ 0.2V or V_{IN} ≥ V_{cc}- 0.2V	-	5.0	-	5.0	-	5.0	-	5.0	mA
		L	***-***	***0.25***	***-***	***0.25***	***-***	***0.25***	***-***	***0.25***	
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	-	0.4	-	0.4	-	0.4	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = - 4 mA	2.4	-	2.4	-	2.4	-	2.4	-	V

Capacitance (f = 1MHz, T_A = 25^0C, V_{cc} = 5V)

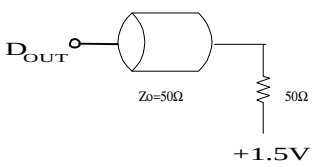
Parameter	Symbol	Test Condition	Maximum	Unit
Input Capacitance	C_{in}	V_{in} = 0V	7	ρF
I/O Capacitance	$C_{I/O}$	V_{in} = V_{out} = 0V	8	ρF

* This parameter is guaranteed by device characterization and is not production tested.

AC Test Conditions

Input Pulse Level Gnd to 3.0V
Input Rise and Fall Times 3ns
Input and Output Timing Reference Level 1.5V

Output Loads



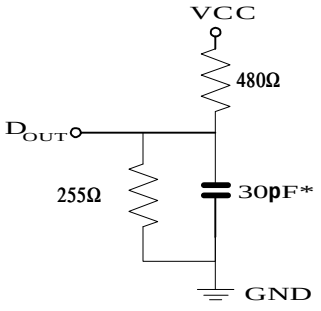


Figure A. Output Load

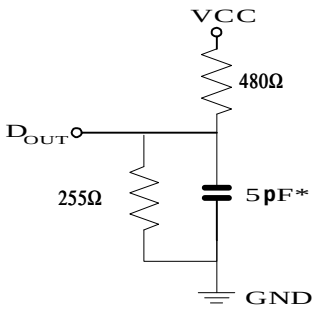


Figure B. Output Load for t_{CLZ} t_{CHZ} t_{OLZ} t_{WHZ} t_{OW} and t_{OHZ}

* Including Scope and Jig.

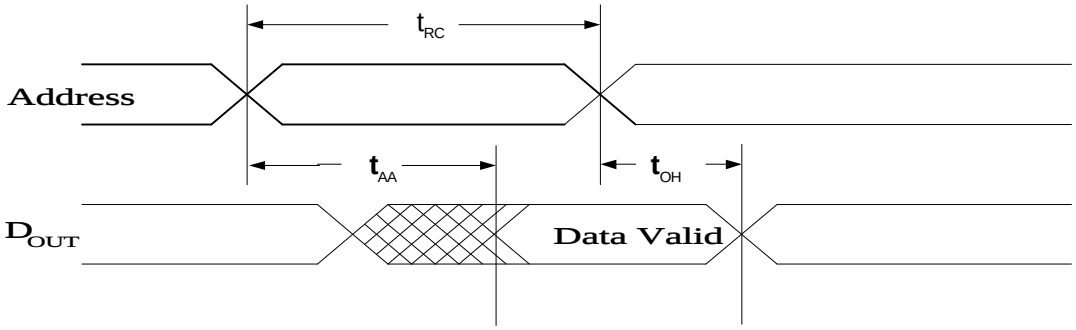
Read Cycle [3,9] (V_{cc} = 5V±5%/10%, Gnd = 0V, T_A = 0^0C to +70^0C)

Parameter	Symbol	-8		-10		-12		-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{RC}	8	-	10	-	12	-	15	-	ns	
Address Access Time	t_{AA}	-	8	-	10	-	12	-	15	ns	
Chip Enable Access Time	t_{ACE}	-	8	-	10	-	12	-	15	ns	
Output Enable Access Time	t_{OE}	-	4	-	5	-	6	-	7	ns	
Output Hold from Address Change	t_{OH}	2	-	2	-	3	-	3	-	ns	
Chip Enable to Output in Low-Z	t_{CLZ}	2	-	2	-	3	-	3	-	ns	4,5
Chip Disable to Output in High-Z	t_{CHZ}	-	2	-	2	-	3	-	4	ns	4,5
Output Enable to Output in Low-Z	t_{OLZ}	0	-	0	-	0	-	0	-	ns	4,5
Output Disable to Output in High-Z	t_{OHZ}	-	2	-	2	-	3	-	4	ns	4,5
Power-Up Time	t_{PU}	0	-	0	-	0	-	0	-	ns	5
Power-Down Time	t_{PD}	-	8	-	10	-	12	-	15	ns	5

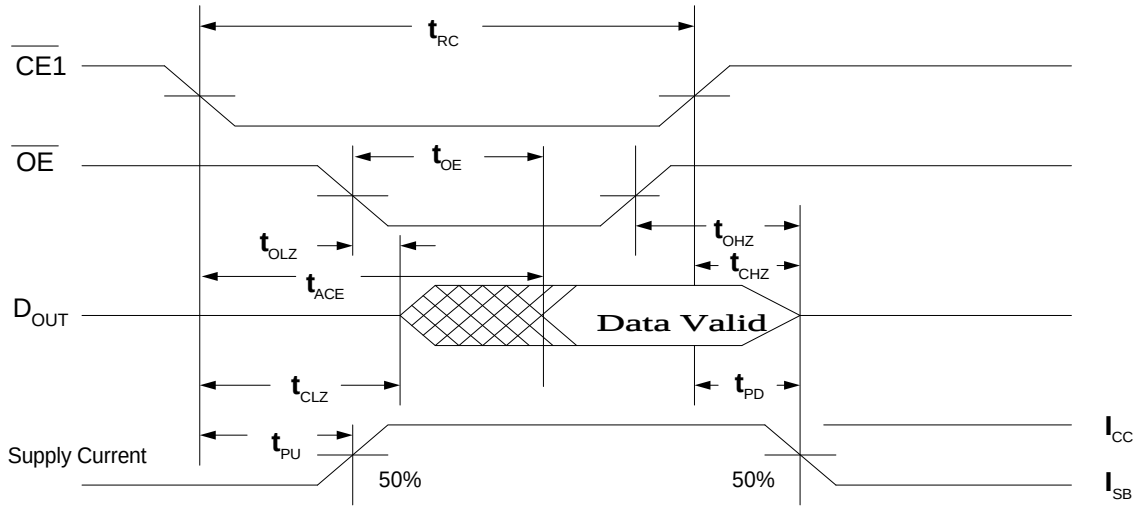
Write Cycle [3,11] (V_{cc} = 5V±5%/10%, Gnd = 0V, T_A = 0^0C to +70^0C)

Parameter	Symbol	-8		-10		-12		-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{WC}	8	-	10	-	12	-	15	-	ns	
Chip Enable to Write End	t_{CW}	7	-	8	-	10	-	13	-	ns	
Address Setup to Write End	t_{AW}	7	-	8	-	10	-	13	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns	
Write Pulse Width	t_{WP}	7	-	8	-	9	-	11	-	ns	
Address Hold from End of Write	t_{AH}	0	-	0	-	0	-	0	-	ns	
Data Valid to Write End	t_{DW}	6	-	6	-	6	-	8	-	ns	
Data Hold Time	t_{DH}	0	-	0	-	0	-	0	-	ns	
Write Enable to Output in High-Z	t_{WZ}	-	5	-	5	-	5	-	5	ns	4,5
Output Active from Write End	t_{OW}	3	-	3	-	3	-	3	-	ns	4,5

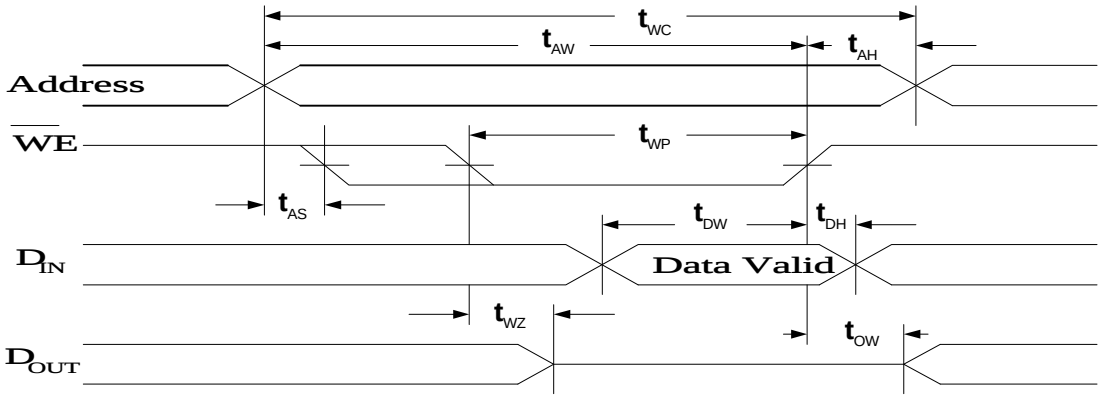
Timing Waveform of Read Cycle (3,6,9) (Address Controlled)



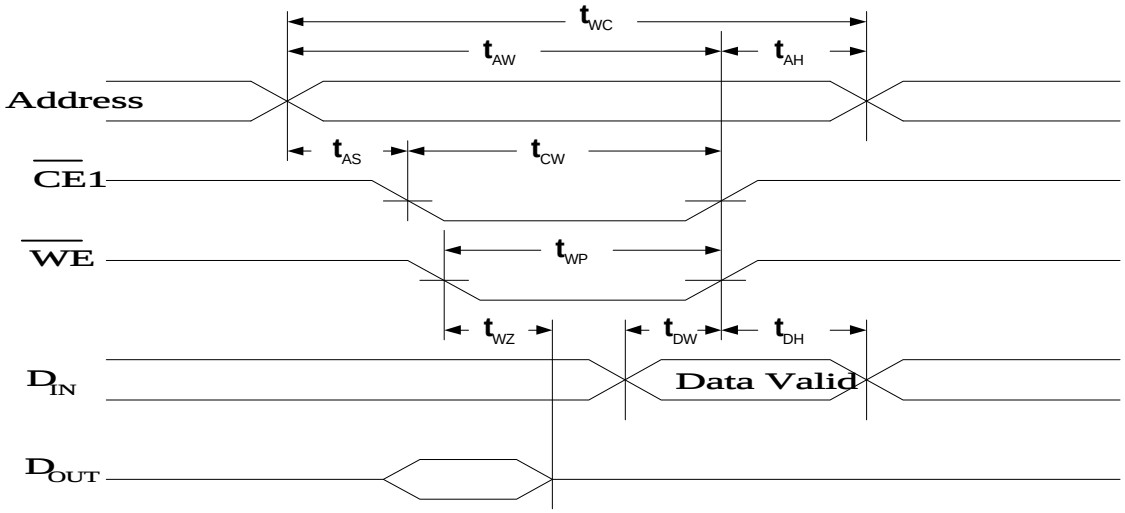
Timing Waveform of Read Cycle (5,6,8,9) ($\overline{CE1}$ Controlled)



Timing Waveform of Write Cycle (10,11) ($\overline{WE}$ Controlled)



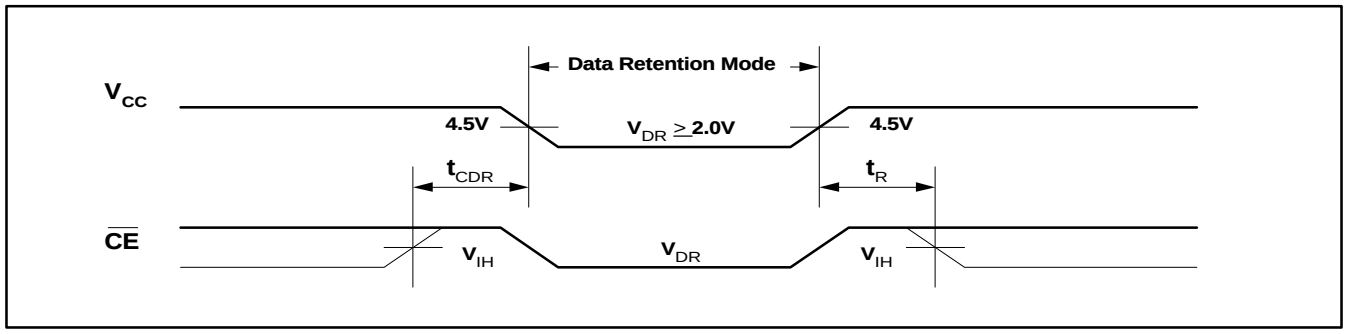
Timing Waveform of Write Cycle (10,11) ($\overline{CE1}$ Controlled)



Data Retention Characteristics (L Version Only)[1]

Parameter	Symbol	Test Condition	Min	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CE}_1 \geq V_{CC}$ - 0.2V	2.0	-	V
Data Retention Current	I_{CCDR}		-	150	µA
Chip Enable to Data Retention Time	t_{CDR}	$V_{IN} \geq V_{CC}$ - 0.2V or	0	-	ns
Operation Recovery Time[2]	t_R	$V_{IN} \leq 0.2V$	t_{RC}	-	ns

Data Retention Waveform (L Version Only)



Notes

1. L-version includes this feature.
2. This Parameter is sampled and not 100% tested.
3. For test conditions, see *AC Test Condition*, Figures A & B.
4. This parameter is tested with CL = 5pF as shown in Figure B. Transition is measured ± 500mV from steady-state voltage.
5. This parameter is guaranteed, but is not tested.
6. $\overline{WE}$ is HIGH for read cycle.
7. $\overline{CE1}$ and $\overline{OE}$ are LOW for read cycle.
8. Address valid prior to or coincident with $\overline{CE1}$ transition LOW.
9. All read cycle timings are referenced from the last valid address to the first transtion address.
10. $\overline{CE1}$ or $\overline{WE}$ must be HIGH during address transitions.
11. All write cycle timings are referenced from the last valid address to the first transition address.

Ordering Information

Device Type	Speed	Package
SD68C32J-10	10 ns	300 mil 28-pin Plastic SOJ
SD68C32J-12	12 ns	
SD68C32J-15	15 ns	
SD68C32J-20	20 ns	
SD68C32LJ-10	10 ns	
SD68C32LJ-12	12 ns	
SD68C32LJ-15	15 ns	
SD68C32LJ-20	20 ns	
SD68C32K-10	10 ns	8x20, 28-pin PlasticTSOP1
SD68C32K-12	12 ns	
SD68C32K-15	15 ns	
SD68C32K-20	20 ns	
SD68C32LK-10	10 ns	
SD68C32LK-12	12 ns	
SD68C32LK-15	15 ns	
SD68C32LK-20	20 ns	