DESCRIPTION

The Hyundai HY5DU663222 is a 67,108,864-bit CMOS Double Data Rate(DDR) Synchronous DRAM, ideally suited for the graphics applications which require frame buffer / texture memory with high bandwidth. HY5DU663222 is organized as 4 banks of 524,288x32.

HY5DU663222 offers fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the clock(falling edges of the $\overline{CLK}$), Data(DQ), Data strobe(DQS) and Write data mask(DM) inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2.

Mode register set options include the length of pipeline ($\overline{CAS}$ latency of 2/3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 2/4/8), and the burst count sequence(sequential or interleave). Because data rate is doubled through reading and writing at both rising and falling edges of the clock, 2X higher data bandwidth can be achieved than that of traditional (single data rate) Synchronous DRAM.

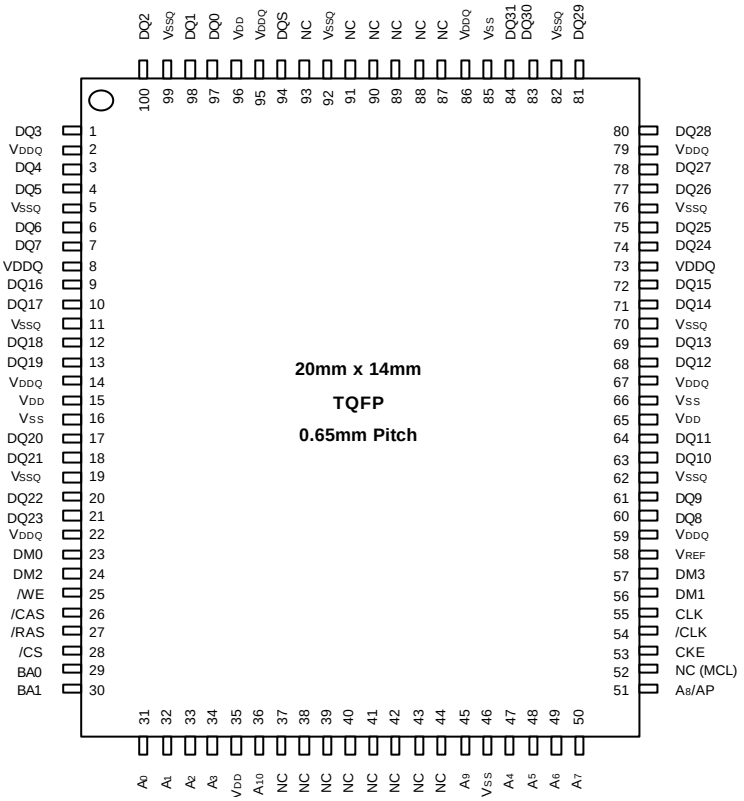
FEATURES

- 2.8V V_{DD} and V_{DDQ} power supply
- All inputs and outputs are compatible with SSTL_2 interface
- JEDEC standard 20mmx14mm 100pin TQFP with 0.65mm pin pitch
- All addresses and control inputs except Data, Data strobe and Data masks latched on the rising edges of the clock
- Data(DQ) and Write masks(DM0~DM3) latched on both rising and falling edges of the Data Strobe
- Data outputs on DQS edges when read (edged DQ)
- Data inputs on DQS centers when write (centered DQ)
- Data strobes synchronized with output data for read and input data for write
- Delay Locked Loop(DLL) installed with DLL reset mode
- Write mask byte controls by DM
- Programmable $\overline{CAS}$ Latency 2 / 3 supported
- Write Operations with 1 Clock Write Latency
- Programmable Burst Length 2 / 4 / 8 with both sequential and interleave mode
- Internal 4 banks operation with single pulsed $\overline{RAS}$
- Auto refresh and self refresh supported
- 2048 refresh cycles / 16ms

ORDERING INFORMATION

Part No.	Power Suppy	Clock Frequency	Organization	Interface	Package
HY5DU663222Q-5	V_{DD} = 2.8V V_{DDQ} = 2.8V	200MHz	4Banks x 512Kbit x 32	SSTL_2	20mmx14mm 100Pin TQFP
HY5DU663222Q-55		183MHz			
HY5DU663222Q-6		166MHz			
HY5DU663222Q-7		143MHz			

PIN CONFIGURATION

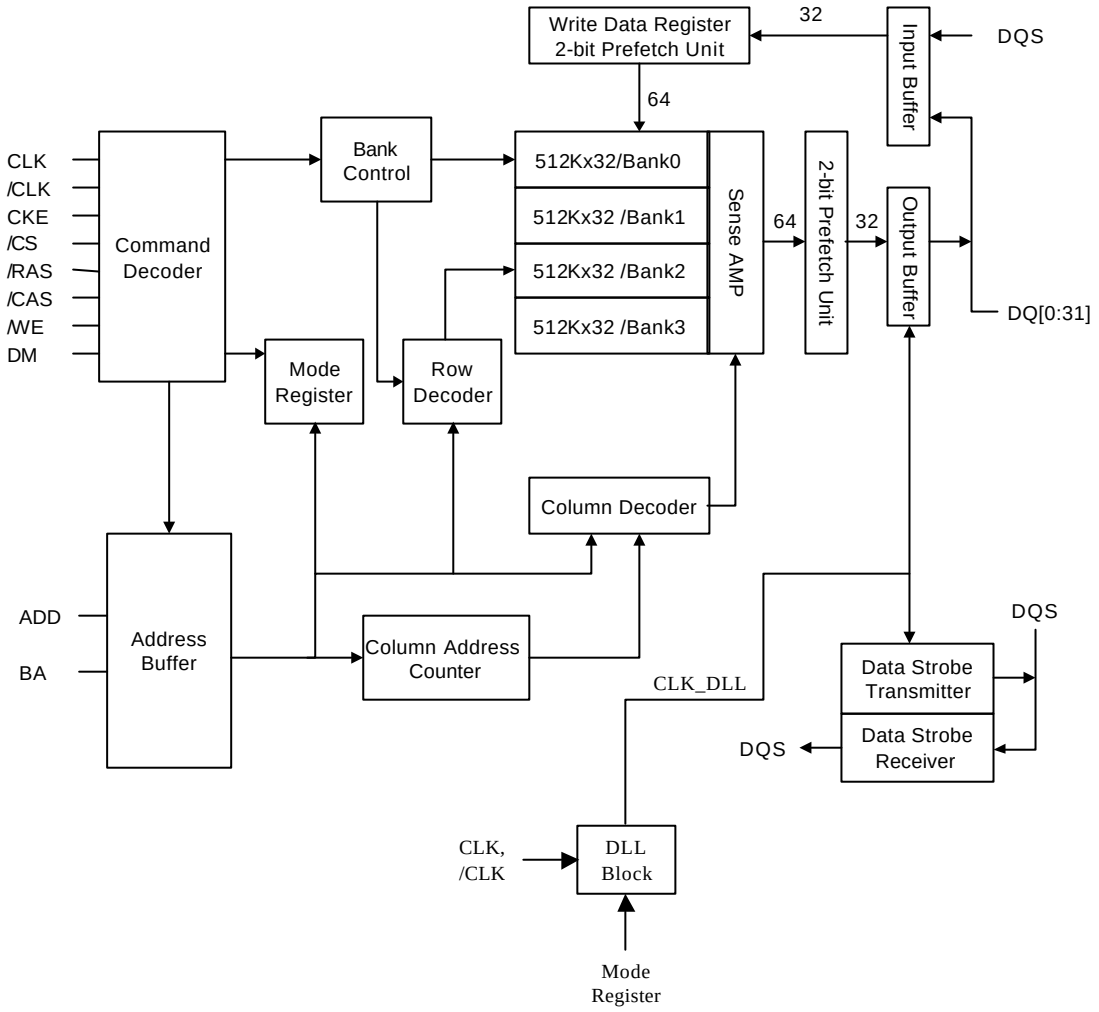


PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK, $\overline{CLK}$	Differential Clock Input	The system clock input. All of the inputs are letched on the rising edges of the clock except DQ, DQS and DM that are sampled on the both.
CKE	Clock Enable	Controls internal clock signal. When deactivated, the SDRAM will be one of the states among power down or self refresh.
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK/ $\overline{CLK}$, CKE, DQS and DM.
BA0, BA1	Bank Select Address	Selects bank to be activated during either $\overline{RAS}$ or $\overline{CAS}$ activity. Selects bank to be read/written during either $\overline{RAS}$ or $\overline{CAS}$ activity.
A0 ~ A10	Address	Row Address : A0 ~ A10, Column Address : A0 ~ A7 Auto-precharge flag : A8
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the command being issued. Refer function truth table for details.
DM0~DM3	Write Mask	Masks input data in write mode.
DQS	Data Input/Output Strobe	Active on the both edges for Data Input and Output.
DQ0 ~ DQ31	Data Input/Output	Bidirectional data input / output pin.
VDD/VSS	Power Supply/Ground	Power supply for internal circuits and input buffers.
VDDQ/VSSQ	Data Output Power/Ground	Power supply for output buffers for Noise immunity.
VREF	Reference Voltage	Reference voltage for inputs for SSTL interface.
NC, (MCL)	No Connection	No connection. (Must Connect Low)

FUNCTIONAL BLOCK DIAGRAM

4banks x 512Kbit x 32 I/O Double data rate Synchronous DRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.5 ~ 3.6	V
Voltage on VDD relative to VSS	VDD	-0.5 ~ 3.6	V
Voltage on VDDQ relative to VSS	VDDQ	-0.5 ~ 3.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	2	W
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability.

DC OPERATING CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VDD	2.66	2.8	2.94	V	
Power Supply Voltage	VDDQ	2.66	2.8	2.94	V	1
Input High Voltage	VIH	VREF + 0.18	-	VDDQ + 0.3	V	
Input Low Voltage	VIL	-0.3	-	VREF - 0.18	V	2
Termination Voltage	VTT	VREF - 0.04	VREF	VREF + 0.04	V	
Reference Voltage	VREF	1.33	1.4	1.47	V	3,4

Note :
1. VDDQ must not exceed the level of VDD.
2. VIL (min) is acceptable -1.5V AC pulse width with ≤ 5ns of duration.
3. The value of VREF is approximately equal to 0.5VDDQ.
4. Peak to Peak AC noise on VREF may not exceed 2% VREF(DC).

AC OPERATING TEST CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Value	Unit
Reference Voltage	VDDQ x 0.5	V
Termination Voltage	VDDQ x 0.5	V
AC Input High Level Voltage (VIH, min)	VREF + 0.35	V
AC Input Low Level Voltage (VIL, max)	VREF - 0.35	V
Input Timing Measurement Reference Level Voltage	VREF	V
Output Timing Measurement Reference Level Voltage	VTT	V

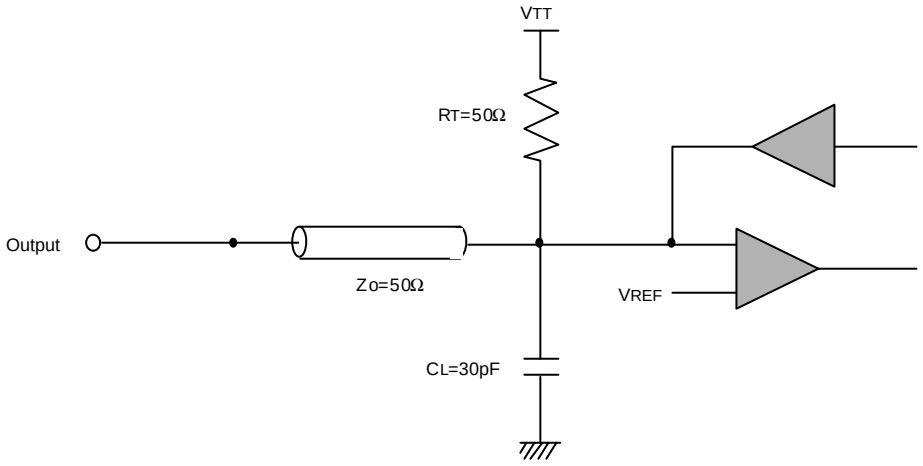
AC OPERATING TEST CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V) *- continued -*

Parameter	Value	Unit
Input Signal maximum peak swing	1.5	V
Input minimum Signal Slew Rate	1	V/ns
Termination Resistor (RT)	50	Ω
Output Load Capacitance for Access Time Measurement (CL)	30	pF

CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Pin	Symbol	Min	Max	Unit
Input Capacitance	A0 ~ A10, BA0 ~ BA1	CIN	2	3	pF
Clock Capacitance	CLK, $\overline{CLK}$, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CCLK	2	3	pF
Data Input / Output Capacitance	DQ0 ~ DQ31, DQS, DM0~3	CIO	4	5	pF

OUTPUT LOAD CIRCUIT



DC CHARACTERISTICS I (TA=0 to 70°C, Voltage referenced to V_{SS} = 0V)

Parameter	Symbol	Min.	Max	Unit	Note
Input Leakage Current	I_{LI}	-5	5	μA	1
Output Leakage Current	I_{LO}	-5	5	μA	2
Output High Voltage	V_{OH}	V_{TT} + 0.76	-	V	I_{OH} = -15.2mA
Output Low Voltage	V_{OL}	-	V_{TT} - 0.76	V	I_{OL} = +15.2mA

Note :
1. V_{IN} = 0 to V_{DD}+5%
2. D_{OUT} is disabled, D_{IN} = 0 to V_{DDQ}+5%

DC CHARACTERISTICS II (TA=0 to 70°C, Voltage referenced to V_{SS} = 0V)

Parameter	Symbol	Test Condition	Speed				Unit	Note
			-5	-55	-6	-7		
Operating Current	I_{DD1}	Burst length=2, One bank active $t_{RC} \geq t_{RC}$(min), I_{OL}=0mA	280	270	260	240	mA	1
Precharge Standby Current in Power Down Mode	I_{DD2P}	CKE ≤ V_{IL}(max), t_{CK} = min	10				mA	
Precharge Standby Current in Non Power Down Mode	I_{DD2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CK} = min Input signals are changed one time during 2clks	60				mA	
Active Standby Current in Power Down Mode	I_{DD3P}	CKE ≤ V_{IL}(max), t_{CK} = min	20				mA	
Active Standby Current in Non Power Down Mode	I_{DD3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CK} = min Input signals are changed one time during 2clks	70				mA	
Burst Mode Operating Current	I_{DD4}	$t_{CK} \geq t_{CK}$(min), I_{OL}=0mA, CL=3.0 All banks active	470	440	410	370	mA	1
Auto Refresh Current	I_{DD5}	$t_{RC} \geq t_{RC}$(min), All banks active	320				mA	2
Self Refresh Current	I_{DD6}	CKE ≤ 0.2V	3.5				mA	

Note :
1. I_{DD1} and I_{DD4} depend on output loading and cycle rates. Specified values are measured with the output open.
2. Min. of tRFC (Auto Refresh Row Cycle Time) is shown at AC CHARACTERISTICS.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-5		-55		-6		-7		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
Row Cycle Time		tRC	60	-	60.5	-	60	-	63	-	ns	
Auto Refresh Row Cycle Time		tRFC	70	-	71.5	-	72	-	77	-	ns	
Row Active Time		tRAS	40	120K	44	120K	42	120K	49	120K	ns	
Row Address to Column Address Delay		tRCD	20	-	16.5	-	18	-	21	-	ns	
Row Active to Row Active Delay		tRRD	2	-	2	-	2	-	2	-	CLK	
Column Address to Column Address Delay		tCCD	1	-	1	-	1	-	1	-	CLK	
Row Precharge Time		tRP	20	-	16.5	-	18	-	21	-	ns	
Write Recovery Time		tWR	10	-	11	-	12	-	14	-	ns	
Last Data-In to Read Command		tDRL	1	-	1	-	1	-	1	-	CLK	
Auto precharge Write Recovery+Precharge Time		tDAL	30	-	27.5	-	30	-	35	-	ns	
System Clock Cycle Time	$\overline{CAS}$ Latency = 3	tCK	5	10	5.5	10	6	10	7	10	ns	
	$\overline{CAS}$ Latency = 2		10	12	10	12	10	12	10	12	ns	
Clock High Level Width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	CLK	
Clock Low Level Width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	CLK	
Data-Out edge to Clock edge Skew (DLL_On)		tAC	-0.7	0.7	-0.7	0.7	-0.75	0.75	-0.75	0.75	ns	
DQS-Out edge to Clock edge Skew (DLL_On)		tDQSCK	-0.7	0.7	-0.7	0.7	-0.75	0.75	-0.75	0.75	ns	
Data-Out edge to Clock edge Skew (DLL_Off)		tAC	4.5	7.0	4.5	7.0	4.5	7.0	4.5	7.0	ns	
DQS-Out edge to Clock edge Skew (DLL_Off)		tDQSCK	4.5	7.0	4.5	7.0	4.5	7.0	4.5	7.0	ns	
DQS-Out edge to Data-Out edge Skew		tDQSQ	-0.5	0.5	-0.5	0.5	-0.5	0.5	-0.5	0.5	ns	
Data/DQS-Out Valid Window		tDV	0.35	-	0.35	-	0.35	-	0.35	-	CLK	
Read DQS Preamble Time		tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	CLK	
Read DQS Postamble Time		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	CLK	
Write DQS Preamble Setup Time		tWPRES	0	-	0	-	0	-	0	-	CLK	
Write DQS Preamble Hold Time		tWPREH	0.25	-	0.25	-	0.25	-	0.25	-	CLK	
Write DQS Postamble Time		tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	CLK	
Write DQS High Level Width		tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	CLK	
Write DQS Low Level Width		tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	CLK	
CLK to First Rising edge of DQS-In		tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	CLK	
Input Setup Time to CLK (ADDR & Control)		tIS	1.1	-	1.1	-	1.1	-	1.1	-	ns	1
Input Hold Time to CLK (ADDR & Control)		tIH	1.1	-	1.1	-	1.1	-	1.1	-	ns	1
Data-In Setup Time to DQS-In (DQ & DM)		tDS	0.5	-	0.5	-	0.5	-	0.5	-	ns	2
Data-in Hold Time to DQS-In (DQ & DM)		tDH	0.5	-	0.5	-	0.5	-	0.5	-	ns	2
DQ & DM Input Pulse Width		tDIPW	1.6	-	1.6	-	1.6	-	1.75	-	ns	
Mode Register Set Delay		tMRD	2	-	2	-	2	-	2	-	CLK	
Power Down Exit Time		tPDEX	10	-	10	-	10	-	10	-	ns	
Exit Self Refresh to Non-Read Command		tXSNR	70	-	71.5	-	72	-	77	-	ns	
Exit Self Refresh to Read Command		tXSRD	200	-	200	-	200	-	200	-	CLK	

Note :

1. Data sampled at the rising edges of the clock : A0~A10, BA0~BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$.
2. Minimum tRC after Self Refresh Exit command, where CKE is held high, is required to complete Self Refresh Exit.

SIMPLIFIED COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	A8/AP	BA	Note
Extended Mode Register Set		H	X	L	L	L	L	OP code			1,2
Mode Register Set		H	X	L	L	L	L	OP code			1,2
Device Deselect		H	X	H	X	X	X	X			1
No Operation				L	H	H	H				
Bank Active		H	X	L	L	H	H	RA		V	1
Read		H	X	L	H	L	H	CA	L	V	1
Read with Autoprecharge									H		1,3
Write		H	X	L	H	L	L	CA	L	V	1
Write with Autoprecharge									H		1,4
Precharge All Banks		H	X	L	L	H	L	X	H	X	1,5
Precharge selected Bank									L	V	1
Read Burst Stop		H	X	L	H	H	L	X			1
Auto Refresh		H	H	L	L	L	H	X			1
Self Refresh	Entry	H	L	L	L	L	H	X			1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	H	H	H				1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				1
Active Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	V	V	V				1
	Exit	L	H	X							1

(H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation)

Note :

1. DM states are "Don't Care". Refer to below Write Mask Truth Table.
2. OP Code(Operand Code) consists of A_{0}~A_{10} and BA_{0}~BA_{1} used for Mode Registering duing Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Prechagre command.
3. If a Read with Autoprecharge command is detected by memory component in CLK(n), then there will be no command presented to activated bank until CLK(n+BL/2+t_{RP}).
4. If a Write with Autoprecharge command is detected by memory compoment in CLK(n), then there will be no command presented to activated bank until CLK(n+BL/2+1+tWR+t_{RP}). Write Recovery Time(tWR) which is also called Last Data-In to Precharge delay (t_{DPL}) is needed to guarantee that the last data has been completely written.
5. If A_{8}/AP is "High" when Row Precharge command being issued, BA_{0}/BA_{1} are ignored and all banks are selected to be precharged.

WRITE MASK TRUTH TABLE

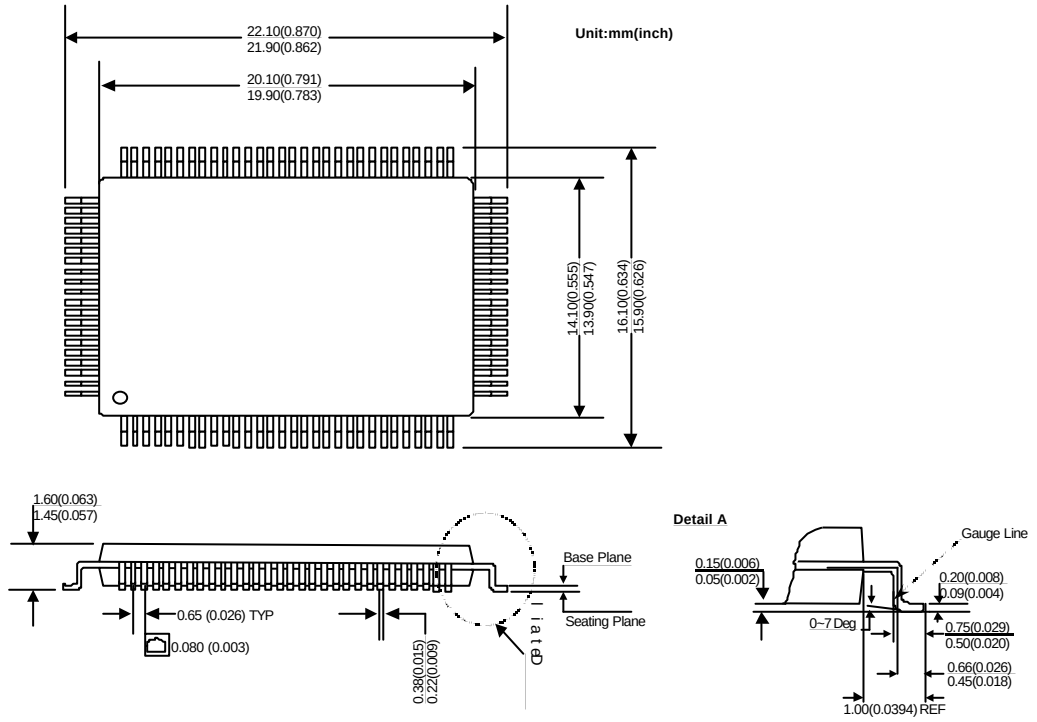
Function	CKEn-1	CKEn	$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	DM 0~3	ADDR	A8/ AP	BA	Note
Data Write	H	X	X	L	X			1
Data-In Mask	H	X	X	H	X			1

Note :

1. Write Mask command masks burst write data with reference to DQS(Data Strobe) and it is not related with read data.

PACKAGE INFORMATION

20mm x 14mm 100pin Thin Quad Flat Package



All dimension in mm (inches). Notation is $\frac{MAX}{MIN}$ or typical.